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A 10-bit 100-MS/s 5.23-mW SAR ADC in 0.18-μm CMOS

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ABSTRACT

A 10-bit 100 MS/s energy-efficient successive-approximation analog-to-digital converter (SAR ADC) is presented in this paper. In order to improve the conversion rate and reduce power consumption as well, a modified spilt-capacitor V_{CM}-based switching scheme is proposed. By utilizing the LSB capacitors to obtain the last-bit, the proposed switching scheme could decrease the area of capacitive DAC. Moreover, by modifying the switching behaviors of the most significant bit (MSB) and 2^{nd}-MSB, the conversion rate could be improved. The prototype SAR ADC fabricated in 0.18 μm CMOS achieves 53.68 dB SNDR and 62.85 dB SFDR at 100 MS/s sampling rate. The active area of the core is 0.216 mm^2. It consumes 5.23 mW with 1.8 V supply, resulting in a Walden figure of merit (FoM) of 123.2 fJ/conversion step.

1. Introduction

Nowadays, successive-approximation (SAR) ADC has drawn a lot of attentions due to its wide usage in many special fields, such as portable electronic systems and wireless sensor networks. Compared with other types ADC, SAR ADCs exhibit the best energy efficiency for medium-to-high speed, moderate-resolution, low-power applications [1,2,17] since the process scaling down. However, it is still difficult to compromise between the speed, resolution and power of SAR ADCs. Increasing speed will cause the decision errors of SAR ADCs which deteriorates the resolution performance. Moreover, the energy per conversion of SAR ADCs is approximately linearly proportional to the resolutions, and when speed is close to upper limit, the power consumption will be greatly increased [3]. Therefore, it is an austere challenge to achieve an appropriate compromise between the specifications of SAR ADC in various applications.

In this paper, a single-channel, single-bit/cycle SAR ADC is designed to boost the conversion rate while maintaining attractive power efficiency. A novel switching scheme based on split-capacitor V_{CM}-based switching is proposed to achieve this goal. The MSB and 2^{nd}-MSB capacitors in digital to analog convertor (DAC) are charged (or discharged) by V_{REF} (or Gnd) instead of V_{CM}, improving the DAC settling speed. In addition, asynchronous clock as well as dynamic SAR logic controller is employed to further increase the conversion speed. The measurement results show that a 10-bit 100 MS/s SAR ADC adopting the proposed techniques achieves a Walden figure of merit (FoM) of 123.2 fJ/conversion step, which is comparable to the state-of-the- art in 0.18 μm CMOS process.

This paper is organized as follows. Section 2 describes the overall ADC architecture. Section 3 presents the proposed switching scheme. In addition, the average switching energy is also analyzed in this section. Section 4 introduces the circuit details including the optimizations of the bootstrapped switch, the comparator and the SAR logic. Section 5 shows the measurement results of the prototype SAR ADC. And section 6 concludes this paper.

2. ADC architecture

Fig. 1 shows the structure of the proposed SAR ADC. In general, it consists of two bootstrapped sampling switches, a differential binary-weighted capacitive DAC, a lower-power dynamic comparator, an asynchronous SAR logic controller and a clock generator. To suppress the supply voltage noise and have good common-mode noise rejection, the fully differential architecture is employed. The input signal is sampled on the top-plate nodes of the capacitor array by bootstrapped switches, and the comparator compares the voltage on the differential capacitor arrays and generates the corresponding digital codes. The output digital codes of comparator are stored in the SAR logic, which in turn feedback the control signals to the DAC switches. The ADC repeats this procedure until all 10 bits are decided.

As shown in Fig. 1, the DAC array is used as the sampling capacitor and its MSB capacitor is split as a sub-array [4]. Therefore, the DAC arrays are composed of two identical sub-DAC arrays, the main sub-array and the MSB sub-array. Due to the usage of top-plate sampling and achieving the LSB-bit by the LSB capacitor (C_{b1} or C_{e1}), the total

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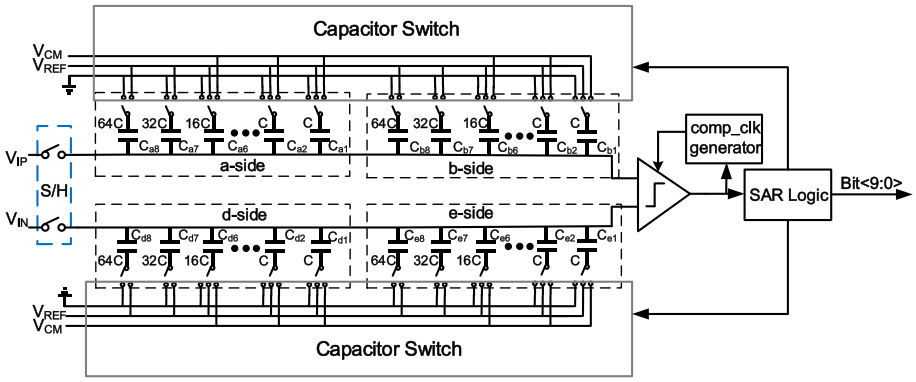

Fig. 1. Block diagram of the SAR ADC.

capacitance is directly reduced by a fraction of four, which can decrease the power consumption and ameliorate the conversion rate. In addition, the asynchronous logic is employed, and the dynamic logic controller makes the optimization of each bit cycle achievable.

3. Modified spilt-capacitor V_{CM}-based switching scheme

3.1. Modified spilt-capacitor V_{CM}-based switching scheme

Compared with the conventional switching scheme, the energy-saving [5], monotonic [6] and V_{CM}-based [7] switching schemes reduce switching energy by 69%, 81% and 90%, respectively. Although V_{CM}-based switching scheme could save power consumption, it is difficult for the CMOS transmission gate to transfer the V_{CM} voltage exactly in a short-time. As a result, the incomplete settling deteriorates the ADC performance [8]. In order to make the proposed SAR ADC achieves the performance of 10-bit 100 MS/s and achieves a better power efficiency, a modified spilt-capacitor V_{CM}-based switching scheme is proposed. The design considerations are illustrated as follows:

a) Because the spilt-capacitor V_{CM}-based switching scheme makes an excellent trade-off between the power efficiency, linearity and the complexity of switching logic [9], it is relatively suitable for us to achieve the expected performance. So we propose a modified switching scheme based on the spilt-capacitor V_{CM}-based switching scheme for the proposed high conversion rate SAR ADC.
b) By the way of achieving the last-bit using the LSB capacitor of the main sub-array, the proposed modified switching scheme could reduce the total capacitance of a single-end to $256C_{unit}$ for a 10-bit SAR ADC, which saves 50% total capacitance compared with the spilt-capacitor V_{CM}-based switching scheme, 75% compared with the conventional switching scheme. It is obvious that the reduced total capacitance makes lower switching energy and the faster settling for DAC capacitors array which benefits for improving the conversion speed of SAR ADCs. The switching energy would be analyzed in the next part 3.2.
c) With the use of V_{REF} and gnd instead of V_{CM} in 2^{nd}-MSB and 3^{rd}-MSB bits in DAC settling, the transmission speed of the reference voltages are greatly improved. Thus the DAC settling time is significantly reduced. Fig. 2 shows the switching procedures for a 3-bit SAR ADC using the conventional split-capacitor V_{CM}-based switching scheme and the proposed switching scheme, respectively.

As shown in Fig. 2 (a) and Fig. 2 (b), when the MSB = 1, the 2^{nd}-MSB = 0 (conditionl) or the MSB = 0, the 2^{nd}-MSB = 1(conditionll), the spilt-capacitor V_{CM}-based switching scheme need to change the voltage of the MSB-capacitance from V_{REF} or ground to V_{CM} to get the 3^{rd}-MSB bit, which would require relatively longer time due to the V_{CM} being 900 mV (a middle voltage). However, the proposed switching scheme doesn't have this process, which could cut down the settling time of the DAC array. Fig. 3 shows the simulated DAC settling behaviors of the two switching scheme. V_P and V_N in Fig. 3 are the voltages on DAC when adopting the spilt-capacitor V_{CM}-based switching scheme. V_{P_M} and V_{N_M} in Fig. 3 are the voltages on DAC when adopting the proposed switching scheme. As shown in Fig. 3, the settling time in conditionlof the proposed switching scheme is decreased by 346.8ps compared to the spilt-capacitor V_{CM}-based switching scheme, which is approximately the worst condition for settling time of DAC capacitors array.

In general, we set the uniform reset time of every comparator according to the worst settling time of DAC capacitors array. So it is obviously that the proposed switching scheme would reduce the time of a period by 3.468 ns (a roughly estimation for a 10-bit SAR ADC). Therefore, the proposed switching scheme in this paper is more suitable for high conversion rate SAR ADC.

As shown in Fig. 2(b), during the sampling phase, the differential input signals are sampled on the top plates of the DAC capacitor array. Meanwhile, the bottom plates of C_{a8}, C_{a7}, C_{e8}, C_{e7} are charged to V_{REF} and C_{b8}, C_{b7}, C_{d8}, C_{d7} are reset to ground, and the others (C_{a6} to C_{a1}, C_{b6} to C_{b1}, C_{d6} to C_{d1} and C_{e6} to C_{e1}) are charged to V_{CM}. Then CLKs triggers the comparator to determine the MSB-bit. The MSB-bit is determined without switching any capacitor by using the top plates sampling technique.

The proposed switching scheme is divided into three parts:

a) For MSB and 2^{nd}-MSB bits: if $V_P > V_N$, C_{a8} (or C_{a7}) is pulled down to ground while C_{d8} (or C_{d7}) is pulled up to V_{REF}. And if $V_P < V_N$, C_{b8} (or C_{b7}) is charged to V_{REF} while C_{e8} (or C_{e7}) is discharged to ground.
b) For 3^{rd}-MSB to 8^{th}-MSB bits: It is the same to the process of capacitance-split V_{CM}-based switching scheme [9].
c) For 9^{th}-MSB bit: if $V_P > V_N$, C_{b1} is pulled down to ground. Otherwise, C_{b1} is charged to V_{REF}.

The explanation of the DAC switch arrangement is given as follows:

(1) V_{CM}-Based switching scheme is very sensitive to the common-mode voltage and the DAC establishment accuracy. In addition, when the capacitance is charged to the V_{CM} voltage, a longer time is required. Therefore, the V_{CM}-based switching scheme is not suitable for MSB in such a high speed SAR ADC. Moreover, the switching scheme using "1" and "0" is not sensitive to the DAC establishment accuracy. So, the MSB and 2^{nd}-MSB bits use the split "1" and "0" switching scheme.
(2) Considering its switching energy is lower, the V_{CM}-based switching scheme is applied for 3^{rd}-MSB to 8^{th}-MSB bits to reduce the power consumption.