Microelectronics Journal 78 (2018) 94–100

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# Static noise margin trade-offs for 6T-SRAM cell sizing in 28 nm UTBB FD-SOI CMOS technology

Fabián Olivera [a,b,*], Antonio Petraglia [a]

[a] Federal University of Rio de Janeiro, EPOLI/PEE/COPPE, Rio de Janeiro, RJ, Brazil
[b] Federal Center for Technological Education Celso Suckow da Fonseca (CEFET/RJ), Nova Friburgo, RJ, Brazil

ARTICLE INFO

*Keywords:*
CMOS memory circuits
Low voltage
Process variation
SRAM
Static noise margin
Sub-threshold operation
Yield

ABSTRACT

In this paper, analytical expressions for the conventional definition of write static noise margin (WSNM) for 6T-SRAM cells at sub-threshold operation are derived. Drain-induced barrier lowering (DIBL) and body-biasing effects are considered in order to achieve an appropriate model for fully depleted silicon-on-insulator (FD-SOI) CMOS technology. By observing the expressions for WSNM and read SNM (RSNM) we introduce an alternative design parameter ($\Gamma$) for 6T-SRAM cell sizing, whose purpose is to control read and write static noise margins simultaneously, thereby providing effective stability balance. This paper also shows that low-leakage cells with suitable stability can be designed by using a non-traditional sizing for 6T-SRAM cells, in which increased transistor lengths are employed to reduce leakage, assisted by a word-line voltage reduction technique to increase read margin. In addition, a statistical analysis for both read and write static noise margins taking into account manufacturing process variations was carried out with the purpose of designing a high-yield 6T cell. Analytical expressions and the designed 6T cell were verified by extensive HSPICE simulations using a 28 nm ultra-thin body and buried oxide (UTBB) FD-SOI CMOS technology.

## 1. Introduction

Due to the growth of internet of things (IoT) industry applications, ultra low power (ULP) has received increasing attention in system-on-chip (SoC) designs owing to the emergence of several circuits that require prolonged battery life [1]. The SRAM cache static leakage current is one of the main causes of power consumption in energy-efficient applications [2,3]. An effective strategy to mitigate such power loss consists of decreasing the supply voltage down to near data retention voltage [4]. The usual metrics to quantify SRAM cell robustness at low supply voltage is the static noise margin (SNM) [5,6], since their positive values allow safe cell operation. Scaling down below 90 nm CMOS process nodes creates a major challenge for designers, as process variability and short channel effects have a strong impact on the minimum supply voltage for proper cell operation [7]. Hence extensive simulations during design stage are required to ensure high yield SRAM cells. Therefore, design methodologies based on analytical models with low computational cost [6] and more efficient simulations [8,9] are very useful in improving time to market. Many analytical models that predict the behavior of hold and read SNM (HSNM and RSNM, respectively) have been proposed in the literature [10,11]. However, to the best of our knowledge, no analytical solution for the conventional write SNM (WSNM) definition [12] has so far been reported in the literature. A conventional model approach for the analysis of read stability and write ability tradeoffs is based on the N-curve [13], which provides some properties of both operation modes but lacks explicit expressions for WSNM and RSNM.

In this paper, we present analytic expressions for WSNM of 6T-SRAM cells in sub-threshold operation. Consequently, we propose an alternative sizing parameter $\Gamma$, which is the product of both pull-up and cell ratios [14,15], and have opposite logarithm dependence between write and read margins. In addition, we show that a low-leakage cell with suitable stability margins can be developed by using a non-traditional sizing approach for 6T-SRAM cell designs, in which the pull-up and pull-down lengths are adequately increased to reduce cell static leakage. In order to provide a robust cell operation, we carry out a statistical analysis based on Monte Carlo simulations for both WSNM and RSNM, considering global and local process variations. The rest of the paper is organized as follows. Section 2 presents the WSNM modeling. Section 3 introduces the sizing parameter $\Gamma$ and proposes a 6T-SRAM sizing

* Corresponding author. Federal Center for Technological Education Celso Suckow da Fonseca (CEFET/RJ), Nova Friburgo, RJ, Brazil.
*E-mail addresses:* folivera@pads.ufrj.br, luis.mederos@cefet-rj.br (F. Olivera), antonio@pads.ufrj.br (A. Petraglia).

https://doi.org/10.1016/j.mejo.2018.06.001
Received 11 October 2017; Received in revised form 22 February 2018; Accepted 4 June 2018
Available online XXX

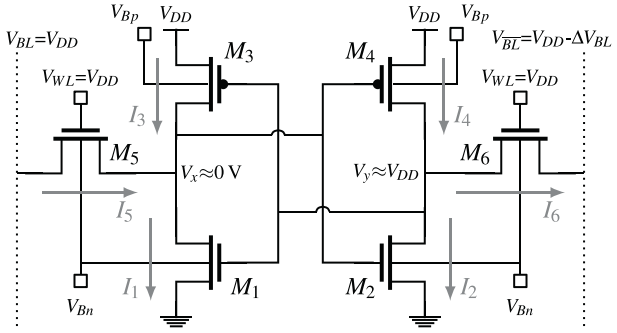


**Fig. 1.** 6T-SRAM cell circuit during write operation.

approach to achieve low-leakage cell designs. Section 4 carries out a sizing exploration in 28 nm UTBB FD-SOI CMOS technology in order to provide a robust cell operation under the manufacturing global process and local mismatch variations. Section 5 presents concluding remarks.

## 2. Write SNM

This section presents an analytical expression for WSNM as a function of both transistor parameters and circuit conditions in write operation. The main motivation is to obtain a transistor sizing relationship between WSNM and RSNM, which can be useful to quantify the effect of transistor dimensions on these noise margins.

### 2.1. Sub-threshold operation

The drain-to-source current of CMOS transistors in sub-threshold operation [11,16] is given by

$$I_{DS} = \frac{W}{L} I_{So} \cdot \exp\left(a_n(V_{GS} - V_T + \lambda V_{DS} + \eta V_{BS})\right) \cdot D(V_{DS}) \tag{1}$$

where $a_n = a/n$, $a = 1/U_T$, $D(X) = 1 - \exp(-aX)$, $U_T$ is the thermal voltage, $n$ the slope factor, $V_T$ is the threshold voltage, $I_{So}$ is the specific current, $W/L$ is the transistor aspect ratio, $\lambda$ and $\eta$ model the DIBL and body bias effects, respectively, and $V_{GS}$, $V_{DS}$ and $V_{BS}$ denote the gate-to-source, drain-to-source and substrate-to-source voltages, respectively.

### 2.2. Write SNM formulation

Fig. 1 shows the 6T-SRAM cell circuit during the write operation, for which it is initially assumed that the internal nodes are retaining the voltages $V_x = 0$ V and $V_y = V_{DD}$, the bit-lines are pre-charged at $V_{BL}=V_{DD}$ and $V_{\overline{BL}} = V_{DD} - \Delta V_{BL}$, respectively, and the word-line is activated by $V_{WL}=V_{DD}$. The DC analysis of this circuit can be decomposed into two inverters ($M_3 - M_1$ and $M_4 - M_2$) loaded by their pass-gate transistors ($M_5$ and $M_6$). The voltage transfer curves $H_1(V_x, V_y)$ and $H_2(V_x, V_y)$ are thus determined, respectively, as

$$H_1(V_x, V_y) : I_3 + I_5 - I_1 = 0 \tag{2}$$

$$H_2(V_x, V_y) : I_4 - I_6 - I_2 = 0 \tag{3}$$

where

$$I_1 = A_1 \exp\left(a_{n1}(V_y + \lambda_1 V_x)\right) D(V_x) \tag{4}$$

$$I_2 = A_2 \exp\left(a_{n2}(V_x + \lambda_2 V_y)\right) D(V_y) \tag{5}$$

$$I_3 = A_3 \exp\left(-a_{n3}(V_y + \lambda_3 V_x)\right) D(V_{DD} - V_x) \tag{6}$$

$$I_4 = A_4 \exp\left(-a_{n4}(V_x + \lambda_4 V_y)\right) D(V_{DD} - V_y) \tag{7}$$

$$I_5 = A_5 \exp\left(-a_{n5}(1 + \lambda_5 + \eta_5)V_x\right) D(V_{DD} - V_x) \tag{8}$$

$$I_6 = A_6 \exp\left(a_{n6}\lambda_6 V_y\right) D(V_y - V_{\overline{BL}}) \tag{9}$$

and

$$A_1 = I_{S1} \exp\left(a_{n1}(\eta_1 V_{Bn} - V_{T1})\right) \tag{10}$$

$$A_2 = I_{S2} \exp\left(a_{n2}(\eta_2 V_{Bn} - V_{T2})\right) \tag{11}$$

$$A_3 = I_{S3} \exp\left(a_{n3}(-\eta_3 V_{Bp} + V_{DD}(1 + \lambda_3 + \eta_3) - |V_{T3}|)\right) \tag{12}$$

$$A_4 = I_{S4} \exp\left(a_{n4}(-\eta_4 V_{Bp} + V_{DD}(1 + \lambda_4 + \eta_4) - |V_{T4}|)\right) \tag{13}$$

$$A_5 = I_{S5} \exp\left(a_{n5}(\eta_5 V_{Bn} + (1 + \lambda_5)V_{DD} - V_{T5})\right) \tag{14}$$

$$A_6 = I_{S6} \exp\left(a_{n6}(\eta_6 V_{Bn} - (1 + \eta_6 + \lambda_6)V_{\overline{BL}} + V_{DD} - V_{T6})\right) \tag{15}$$

where $I_{Si} = (W_i/L_i)I_{Soi}$, for $i = 1, 2, \ldots, 6$, and $V_{Bn}$ and $V_{Bp}$ are the substrate-to-ground voltages of N-type and P-type transistors, respectively. The conventional WSNM [12] is defined as the width of the smallest embedded square plotted between the curves $H_1$ and $H_2$ as illustrated in Fig. 2(a). The square width value can be found once we achieve an analytical solution for the coinciding point ($P_0$) between $H_1$ and $H_2$ (see Fig. 2(b)), because, according to [17], a DC noise voltage ($V_n$) is added to the threshold voltages. The analytical solution of the coinciding point is a mathematical challenge and some approximations

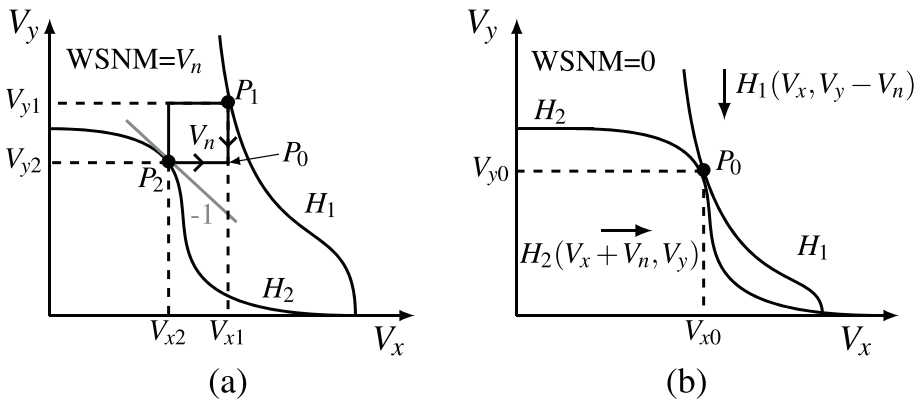


**Fig. 2.** Conventional write static noise margin: (a) smallest embedded square (b) coinciding point.