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Multi stage OTA design: From matrix description to circuit realization

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ABSTRACT

This paper presents a comprehensive approach to frequency compensating multistage amplifiers. Different stage cases have been considered namely, differential voltage and current blocks, and general compensation blocks for both voltage and current states. Then, a matrix description has been proposed to describe the configurations. The approach involved binary matrixes in order to model amplifiers with feedback networks. Evolutionary algorithms were used to find optimum numerical values and simplify symbolic transfer functions. Also a diagram-based design was used to find the appropriate MOSFET DC bias conditions and dimensions. Note that using simplified transfer functions to symbolically locate the poles and zeroes allowed a better circuit design knowledge compared to numerical approaches. To demonstrate the proposed procedure, two circuit were designed in TSMC 0.18 μm CMOS technology and simulated results successfully compared to linear models extracted from the matrix description. According to simulations, the proposed configurations in both voltage and current states show excellence performance versus previous works. Finally, special design cases such as multi-compensation blocks and N-stage approach were discussed.

1. Introduction

With recent advancements in scaling down of CMOS technology and circuit fabrication, demands for high-gain amplifiers have been critically raised. Multistage amplifiers are particularly targeted and three-stage Operational Transconductance Amplifiers (OTAs) are becoming common options [1–5]. However, these circuits need frequency compensation to avoid instability and pole-separation techniques should be used to enhance frequency response [6–15].

Nested Miller Compensation (NMC) technique exploits the double Single Miller Compensation (SMC) by increasing the amplifier stage number; with two nested feedback loops, poles separation can be occurred. Though, this method implies a drastic bandwidth reduction and high power consumption [1,2]. Also NMC shows conditional stability due to the existence of Right Half Plane (RHP) zero. To cancel this undesired zero effect, the NMC with Nulling Resistor (NMCNR) approach was developed [2,4]. The Double Pole Zero Cancellation (DPZC) technique removes two non-dominant poles with two zeros, leading to significant frequency response improvements while the Multipath Nested Miller Compensation (MNMC) method, which adds a stage between the input and second stage, boosts the bandwidth but at the expense of higher power dissipation [5], thus improving the Gain Band-Width product (GBW) but also significantly increasing the circuit complexity. Reversed NMC (RNMC) techniques demonstrate better frequency response due to their insensitivity to load capacitor from the inner compensation loop. So the inner loop is intrinsically stable. All the above techniques, as well as other approaches such as Nested G_m Capacitance Compensation (NGCC) [6], Damping Factor-Control Frequency Compensation (DFCFC) [7], Active Feedback Frequency Compensation (AFFC) [8], or AC Boosting Compensation (ACBC) [9], try to enhance the frequency response parameters such as GBW and Phase Margin (PM) using feedbacks and feed forward paths.

For instance, the circuit shown in Fig. 1 is based on the RNMC technique. This configuration shows that C_L and $C_{c2}$are independent, leading to improved frequency response parameters such as GBW and PM while consuming same power as NMC. The reason is that the pole related to the output is independent from the inner loop. The compensation network in this approach includes two capacitors, which form the feedback and feed

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Abbreviations

ACBC	AC Boosting Compensation;
AFFC	Active Feedback Frequency Compensation
DPZC	Double Pole Zero Cancellation
DFCFC	Damping Factor-Control Frequency Compensation
FF	Fitness Function
FOM	Figure of Merit
GA	Genetic Algorithm
GBW	Gain Band Width
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MNMC	Multipath Nested Miller Compensation
NMC	Nested Miller Compensation
NMCNR	Nested Miller Compensation using Nulling Resistor
NGCC	Nested G_m Capacitance Compensation
NMOS	N-channel MOSFET
OTA	Operational Transconductance Amplifier
PMOS	P-channel MOSFET
PM	Phase Margin
RNMC	Reversed Nested Miller Compensation
RHP	Right Half Plane
Reference Value	RV
SMC	Single Miller Compensation
SR	Slew Rate.

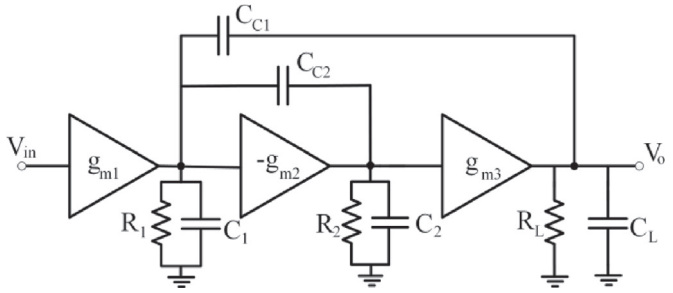

Fig. 1. RNMC configuration.

forward paths.

In Ref. [10], the authors presented a differential voltage block implementation of a compensation network via a single compensation capacitor of small value. A usual differential pair plays the role of a compensation network and forms a differential feedback path. The signs of the differential block inputs must be set according to the negative loops for the compensation capacitor. This guarantees proper Miller effect.

It is important to state that the differential block gain controls the compensation capacitor value. This physically means that smaller OTAs can be achieved, accepting more power consumption due to the larger gain of the differential block. According to the voltage mode, a differential block is used in Ref. [11] as current subtractor to create a compensation network. In Ref. [11], since the inputs of the subtractor have low impedances, the compensation capacitors have been connected to these inputs. This makes the design robust due to the subtractor DC isolation from main circuit [12]. In addition [13] reported a three stage design with both input and output differential stage while second stage is single input. The output differential stage forms both compensation path and DC gain path simultaneously. The exploited structure in Ref. [13] demonstrated an unconditional stability with single and small compensation capacitor. All of mentioned techniques and configurations are compensated via feedbacks and feed forwards paths. These paths usually consist of Miller capacitor, nulling resistor, voltage buffer, current buffer and differential blocks [14,15].

Fig. 2 exhibits an overview of the paper and summarized work flow. In Section 1-1, the matrix [K] is introduced and explained as a description of the amplifier's main part. This matrix identifies the main nodes and the number of symbolical equations. In Section 1–2, the general blocks of compensation are identified in terms of schematic and circuit. Section 2 explains the proposed design, which is described as binary matrixes. In Section 2.1, numerical values are attributed to the parameters of the *Transfer Function* (TF) using a genetic algorithm. Also, section 2-2 addresses the implementation of the proposed schemes accordance to a curve-based approach. Using this approach, the length and the widths and bias voltages of the transistors are obtained. In the third section, the simulation results for different load capacitors are presented, and verified parameters are compared to the similar work in Table 3. How to simplify the TF using another genetic algorithm is explained in Section 4. In this section, for the two proposed methods, TF and circuit dynamics, including poles and zeros, are presented. Additional discussions are presented in Section 5, which include the use of multiple compensating blocks, class n methods, and the creation of loops using differential blocks. Finally, the conclusions are presented in Section 6.

1.1. Matrix description

Let [K]be a binary matrix that models the OTA; its size being depended on the circuit architecture. For instance, each stage can be fully differential or single input-output, as shown in Fig. 3. The connection status between two nodes is modeled by corresponding binary elements. Applying Kirchhoff's Current Law (KCL) at circuit nodes results in a system of equations. Which number of equations depends on the size of [K]. The TF can easily be derived from these equations, given that TF is the ratio of output to input voltages equal to K_n/K_0.

The equations of a fixed structure can be expressed in terms of transconductances, resistors and capacitors. For example at K_2 node, we have:

$$g_{m1} \times K_0 + \frac{K_2}{R_1} + K_2 \times C_1 \times s + A = 0 \tag{1}$$

Where '*s*' is the Laplace variable and '*A*' *is* an expression which elements are related to the probable compensation network. Interestingly, fixed terms are almost represented by a simple pattern:

$$KCL\ at\ i^{th} node : g_{m_{i-1}} \times K_{i-2} + \frac{K_i}{R_i} + K_i \times C_i \times s = 0 \tag{2}$$

So the fixed terms are described by uniquely exploiting [K]. Rewriting the KCL equations according to [K], leads to the following format for the circuit shown in Fig. 3 (with the number of nodes n = 6):

$$[\mathrm{K}]_{n\times n} \times [\text{Fixed Terms}]_{n\times 1} + [A]_{n\times 1} = 0 \tag{3}$$

$$\begin{matrix} V_{in} \\ K_1 \\ K_2 \\ K_3 \\ K_4 \\ K_5 \\ K_6 \end{matrix} \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}_{6\times 6} \times \begin{bmatrix} g_{m1} \times V_{in} + \frac{K_1}{R_1} + K_1 \times C_{11} \times s \\ g_{m1} \times V_{in} + \frac{K_2}{R_1} + K_2 \times C_{12} \times s \\ g_{m2} \times K_2 + \frac{K_3}{R_2} + K_3 \times C_{21} \times s \\ g_{m2} \times K_2 + \frac{K_4}{R_2} + K_4 \times C_{22} \times s \\ g_{m3} \times K_4 + \frac{K_5}{R_3} + K_5 \times C_{31} \times s \\ g_{m3} \times K_4 + \frac{K_6}{R_3} + K_6 \times C_{32} \times s \end{bmatrix}_{6\times 1} + [A]_{6\times 1} = 0 \tag{4}$$