Microelectronics Journal 76 (2018) 43–51

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 1V 1.4 mW multi-band ZigBee receiver with 64 dB SFDR

Zhiqun Li *, Yan Yao, Zengqi Wang, Guoxiao Cheng, Lei Luo

Institute of RF-& OE-ICs, Southeast University, Nanjing 210096, PR China

ARTICLE INFO

Keywords:
ZigBee receiver
Low voltage
Low power
RF front-end
Complex band-pass filter (CBPF)
Limiting amplifier

ABSTRACT

A low voltage low power receiver supporting 780/868/915/2400 MHz ZigBee bands is presented in this paper. The receiver exploiting low-IF architecture consists of a RF-to-BB (baseband) current reuse front-end, a Gm-C based variable gain complex band-pass filter (CBPF) for image rejection and four stages of limiting amplifiers which saturate IF signal for demodulation. The proposed ZigBee receiver chip is implemented in TSMC 180 nm CMOS technology with metal-insulator-metal (MIM) capacitors. PCB measurement results show that the receiver has 45.9 dB conversion gain, 8.5 dB NF and −33.5 dBm out-of-band IIP3 at sub-GHz bands. When working in 2.4 GHz band, the gain is 38.4 dB, noise figure (NF) is 16.7 dB and the out-of-band IIP3 is −28.2 dBm. The S_{11} bandwidth ($S_{11} < -10$ dB) can cover the entire ZigBee spectrum (700–2500 MHz). The receiver consumes 1.42 mW from a 1 V DC supply and the die size is 1.41 mm^2 including all pads.

1. Introduction

Recently, the ZigBee technique based on IEEE 802.15.4 standard has been widely used in power sensitive applications with low rate and low cost, such as wireless sensor networks (WSN). The ultra-low-power (ULP) RF transceiver technology is the key to realize WSN systems as low power consumption is one of the important trends in the development of WSN.

For vanishing power consumption without sacrificing high circuit performance, a popular technique seems to be current reuse among different function modules. Literature [1] presented a quadrature RF receiver where, in a single stage, low-noise amplifier (LNA), mixer and voltage-controlled oscillator (VCO) share the same bias current. However, it is difficult to optimize the noise figure (NF) of LNA and the phase noise of VCO simultaneously due to the same bias current. Moreover, the input match and NF are sensitive to the off-chip inductor, which offers passive pre-gain and narrowband input match. In Ref. [2], a sliding-IF receiver architecture was proposed with a suitable LO frequency plan which completely eliminates the need for a PLL by directly dividing down the fixed oscillator frequency generated by off-chip thin-film bulk-acoustic-wave (BAW) resonator. Thus, the overall power consumption of the receiver is greatly reduced. Current reuse technology is also exploited in the design to further reduce the power consumption of LNA and mixer. In Ref. [3], a low power 2.4 GHz ZigBee receiver employing zero-IF architecture was implemented. In order to reduce the influence of low-frequency flicker noise on the baseband useful signal, the down-converted mixer adopted the passive switching structure which achieves relatively low noise figure. Literature [4] presented a low power 2.4 GHz receiver with a filter capable of tuning the bandwidth for multi-band/multi-standard applications. Amplifier-mixer-filter current-reuse and a BAW resonator are exploited for power solution. However, the NF and IIP3 of the receiver are not easy to be optimized. The research and design on low-power ZigBee RF receiver system integration are mostly concentrated in the 2.4 GHz band [1]- [4], while little attention is paid to sub-GHz band research [5] and no research results covering sub-GHz and 2.4 GHz band have been reported.

This paper shows an implementation of a low power multi-band ZigBee receiver. Details on design and optimization method are provided. A novel graphical method is utilized for the optimization of the conversion gain, NF, input matching and the power consumption of the receiver front-end simultaneously. A novel design method based on poles construction is employed for the implementation of the complex band-pass filter (CBPF) to simplify the circuit structure and cut down the power consumption greatly. The paper is organized as follows. Section 2 describes the ZigBee receiver architecture chosen in this work including module division and link budget. In section 3, key building blocks of the receiver and coexistence considerations are presented. Section 4 shows the measurement results and summarizes the implementation results. Finally, section 5 concludes the paper.

* Corresponding author.
E-mail address: zhiqunli@seu.edu.cn (Z. Li).

https://doi.org/10.1016/j.mejo.2018.04.011
Received 4 March 2018; Received in revised form 8 April 2018; Accepted 17 April 2018

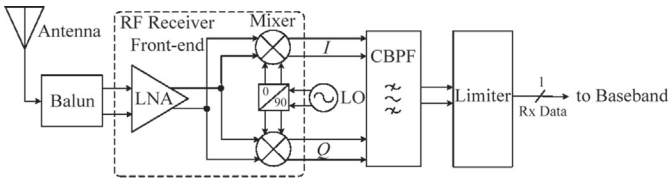

Fig. 1. Block diagram of the multi-band ZigBee RF receiver.

2. ZigBee receiver architecture

2.1. ZigBee receiver architecture

Fig. 1 presents a simplified block diagram of the multi-band ZigBee receiver implemented in this work, including a current reuse front-end which contains the LNA and mixer, the CBPF and a limiting amplifier. A divide-by-2 frequency divider is employed to generate I/Q LO signals for testing. Low-IF architecture is chosen for the receiver with the advantages of high integration level and low cost compared with heterodyne structure and relatively small DC offset and.

1/f noise compared with zero-IF structure. The receiver employs a fully differential circuit structure to reduce the influence of power supply and ground bonding wires utilizing the AC virtual ground feature of differential circuit, with an off-chip balun splitting the RF signal from the antenna. The differential signals are then amplified through LNA and multiplied with I/Q LO signals in the orthogonal inverter mixer to generate I/Q IF signals. Then, the channel selection for 2 MHz IF signal is completed by CBPF, which can also suppress mirror interference [6]. In this design, the spread symbols are specified by using offset quadrature phase-shift keying (O-QPSK) modulation which is possessed of the property of constant envelope. That means the signal amplitude does not contain any useful information. Thus the IF signal selected by CBPF can be sent directly to the limiting amplifier for saturation amplification and conversion to digital signals, which can minimize the complexity and power consumption of the receiver. The digital baseband circuit can then process the signal directly to extract the phase information and complete signal demodulation [7].

2.2. System consideration

According to IEEE 802.15.4 standard, the RF receiver sensitivity P_{sen} must be better than −85 dBm, the maximum input signal power $P_{in,max}$ is −20 dBm, and the packet error rate (PER) should be less than 1% [8]. To

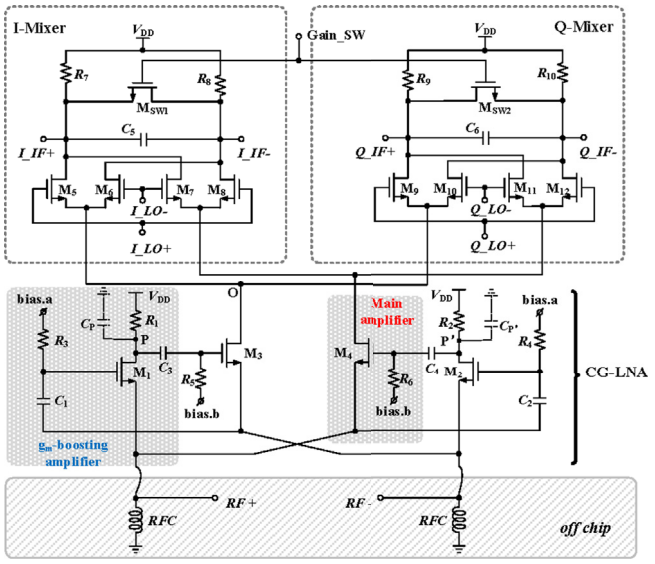

Fig. 3. Schematic of the receiver front-end using LNA-mixer current-reuse structure.

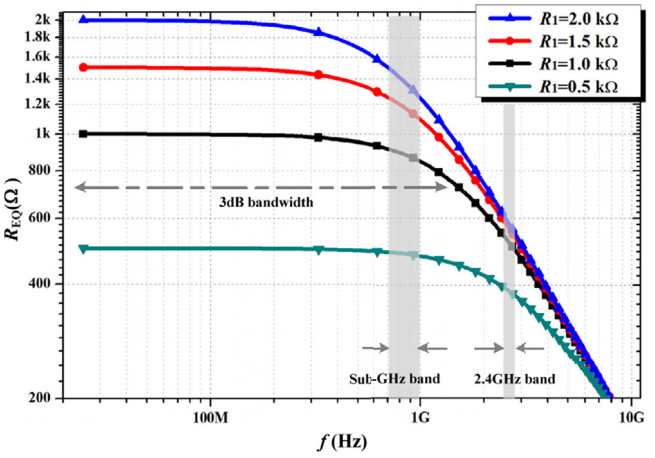

Fig. 4. The equivalent load impedance R_{EQ} of the g_m-boosting amplifier against R_1 and working frequency f.

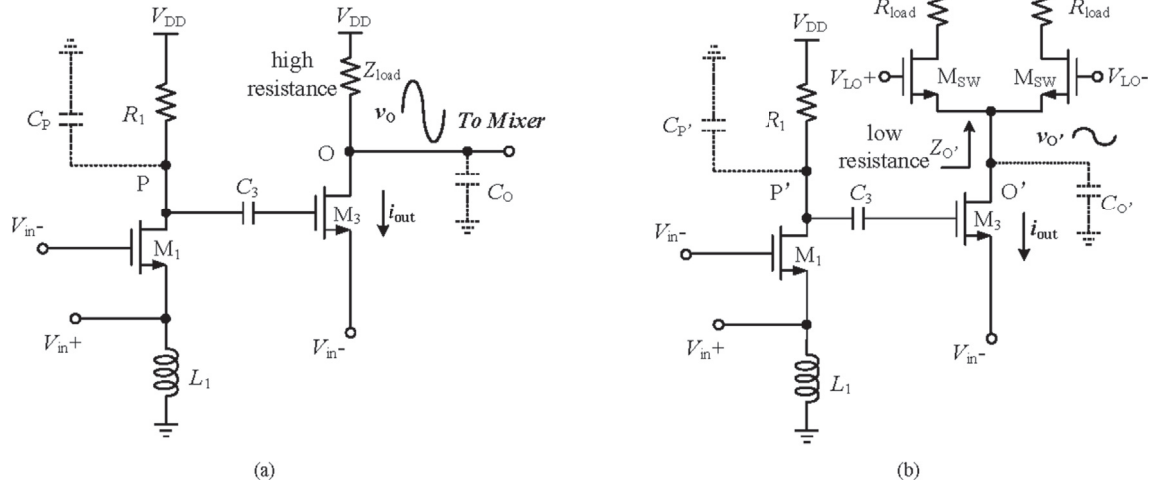

Fig. 2. The receiver front-end using (a) traditional LNA-mixer cascade structure (b) LNA-mixer current-reuse structure.