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A high performance dual clock elastic FIFO network interface for GALS NoC

Seyed Mohamad Taghi Adl [a], Siamak Mohammadi [a,b,*]

[a] Dependable System Design Lab, School of ECE, University of Tehran, Tehran, Iran
[b] School of Computer Science, Institute of Fundamental Sciences (IPM), Tehran, Iran

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ABSTRACT

A dual clock register based elastic First-In First-Out Architecture is presented for Globally Asynchronous Locally Synchronous (GALS) Network on Chip interface. The FIFO is designed using synchronous elastic methods, facilitating its synthesis with commercial CAD tools. This FIFO supports arbitrary phase and frequency for read and write operations and prepares safe data transmission between different clock domains. The presented structure can be easily used as an interface between synchronous or asynchronous GALS modules. The FIFO is simulated and analyzed with 32 nm PTM library in HSPICE. Metastability, process variation, throughput, power, area, delay and maximum frequency are analyzed. Results show elastic FIFO power delay product (PDP) is 23% less than similar synchronous FIFOs. Our proposed elastic FIFO has double capacity while the area is almost the same. The elastic FIFO tolerates better high variability and can preserve its functionality by 5% in average more than the DSPIN synchronous FIFO in presence of variation.

1. Introduction

Increased use of Large Network on Chips (NoC) and spread of complicated System on Chips (SoC) have caused the clock distribution to become a big concern in digital system design [1]. Thereby, designers are forced to use globally asynchronous locally synchronous (GALS) NoC structure [2] for large designs due to its particular characteristics. In GALS structures, each module can operate with its own clock frequency, thus the clock distribution problem can be nearly settled down. However, the communication between two modules with different clock domains will not be as simple as synchronous design communication.

Data transmission between different clock domains may cause metastability problem [3]. As neighboring modules do not have any knowledge of the clock edge of other modules, they cannot know when data is stable and ready to be captured. A FIFO is used as one of the most basic and common methods to solve data transfer dilemma for GALS NoCs [4]. FIFOs are responsible for metastability resolution, while they do not degrade the throughput of the overall system much. Various designs have been presented for GALS network interfaces based on FIFO. All of these designs are comparable in terms of area, power consumption, delay, throughput and robustness against process and environmental variations.

We can categorize presented GALS network interfaces based on FIFO in two main groups, asynchronous FIFOs and synchronous dual clock FIFOs. Both asynchronous and synchronous designs in addition to their circuit features, profit from their design method intrinsic characteristics. Asynchronous FIFOs can tolerate variation better [5]; however handshaking delay over a transaction may degrade the overall system performance [6], while synchronous FIFOs are CAD compatible and can be easily designed and tested with the entire GALS NoC's modules together [7]. Moreover, synchronous modules simply connect to a synchronous FIFO, where asynchronous FIFOs need extra wrapper to convert control protocols [8].

Meanwhile, a new circuit design paradigm, called elastic, has been presented that can benefit from asynchronous circuit advantages in presence of clock signal which is compatible with general CAD tools [9]. The accuracy of clock signal in elastic design is not as important as in synchronous structures [10], and elastic circuits can tolerate clock skew well. Elasticity concept is introduced with various titles in literature, such as latency insensitive [11], or synchronous elastic circuits [12].

In this paper we propose a high performance dual clock elastic FIFO to be used in a GALS NoC network interface. We mainly focus on synchronization function of network interface and do not consider standard interface protocols as in Ref. [13] or [14]. The presented FIFO has simple and efficient design using elastic circuit's capabilities. The FIFO has double capacity, and its dual clock is well designed for GALS structures and works truly with different phase and frequency of read/write clocks. Two designs for this FIFO have been recommended. One is suited for a

* Corresponding author. Dependable System Design Lab, School of ECE, University of Tehran, Tehran, Iran.
E-mail addresses: t.adl@ut.ac.ir (S.M.T. Adl), smohamadi@ut.ac.ir (S. Mohammadi).

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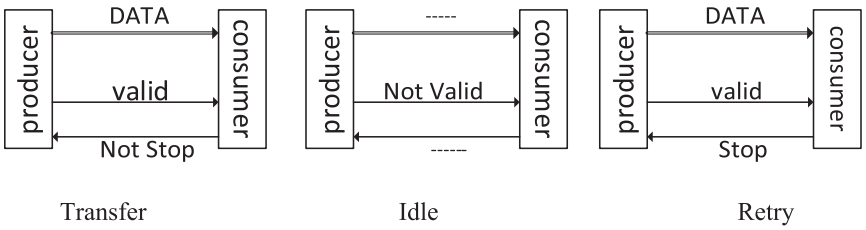

Fig. 1. Three different SELF protocol states [15].

faster writing than reading and the other is when the reading is faster. Our dual clock elastic FIFO is easily connected to synchronous, asynchronous and elastic circuit's interfaces. The presented FIFO is compatible with general CAD tools and there is no need for custom cell designs. The obtained results demonstrate the presented dual clock elastic FIFO consumes less power, while it possesses double data capacity compared to similar structures. The FIFO can be used in higher frequency and shows better resilience against high variation situation.

From the structural point of view, the main contributions of this paper can be expressed as follows:

- The elastic FIFO is simple and has double data capacity in less area than the most similar synchronous dual clock FIFO designs.
- The presented structure benefits from fast, accurate, and efficient full/empty detection mechanism.
- Our FIFO does not need multi-bit synchronization which is complicated and unreliable, but instead uses simple single bit brute-force synchronizer
- The presented dual clock elastic FIFO can easily connect to synchronous, asynchronous, and elastic interfaces

In the following section, some related works are explained. In Section 3 we present the new FIFO structure. In Section 4, the evaluation results are presented and finally the paper is concluded in Section 5.

2. Related work

In this section, some basic information and definitions necessary for the following sections are given. Elasticity concepts will be described first. Afterward, GALS synchronization challenges are explored and some main dual clock FIFO structures will be explained.

2.1. Elastic circuits

According to Cortadella studies, the notion of elasticity belongs to a range of circuit design that can tolerate variable latency inputs and still preserves functionality [16].

In this case synchronous systems are the least elastic designs and delay insensitive asynchronous circuits are the most elastic structures. The new method that is called synchronous elastic design, stays somewhere in the middle of this range. Plenty of properties have been stated for synchronous elastic circuits on computational circuits [17]. We evaluate synchronous elastic circuits for GALS NoC interfaces in this study.

Elastic circuits can preserve functionality while their inputs have arbitrary delays. A storage structure in elastic circuits which is called Elastic Buffer (EB), unlike a flip flop in synchronous design, can hold two distinct data in its two adjacent latches. Since elastic circuits operate with clock, these circuits do not need special interface to communicate with synchronous modules of GALS NoC.

Different structures have been presented for elastic concept [18, 19]. In this paper, we use the synchronous elastic structure presented by Cortadella [15]. Valid and stop signals along with clock form an elastic channel that controls flow of data using SELF protocol. *Valid* control signal is sent in the same direction as data showing its validity. *Stop* control signal is transmitted in the opposite direction of data flow. Inactivity of *stop* signal means the consumer can get new data.

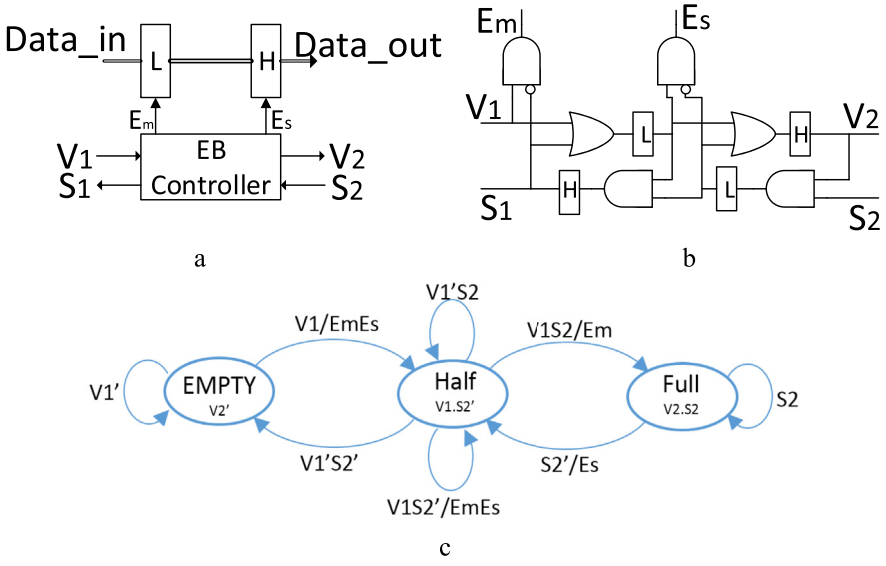

Fig. 2. Elastic buffer [16]. (a) Structure. (b) Controller Structure. (c) Three possible states of buffer.