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# A low power and high gain current-reused LNA using cascaded L-type input matching network

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ABSTRACT

A wideband 2–3 GHz three-stage low noise amplifier (LNA) featuring current reuse, cascaded L-type input matching network (IMN), and optimized multiple gated transistors method (MGTR) using 0.18-$\mu$m CMOS technology is presented in this paper. The current-reused topology is employed in the first two stages to reduce power consumption. For a wideband input matching, the common gate (CG) topology is adopted. Moreover, the cascaded L-type IMN composed of two single L-type networks cascaded in series is proposed for the first time. To improve the linearity performance, the optimized MGTR taking both transconductance $g_m$ and third-order nonlinear coefficient $g_m''$ into consideration is proposed and applied to the output stage. The proposed LNA presents a maximum power gain of 28.0 dB, an input matching across 1.8–5.8 GHz and a high third-order input intercept point ($IIP_3$) of −9.89 dBm. A noise figure (NF) of 3.1–3.5 dB is obtained in the required band with a power dissipation of 6.49 mA from a 3 V power supply.

## 1. Introduction

A low-noise amplifier (LNA) is one of the key building blocks in a typical wireless receiver. Therefore, it needs to meet various design requirements such as low noise figure (NF), low power consumption, high gain, high linearity and wide bandwidth. However, it is difficult to find a common strategy which can fulfill all the desired performance because of the existing contradiction between requirements, such as the contradiction between low noise figure and high linearity. Therefore, a trade-off should be made while designing an LNA.

Based on the input matching and noise performance, two major topologies are used in the LNA architectures, the common source (CS) and the common gate (CG) topology. Compared with the former, the CG topology offers wideband input matching and is less affected by process variations [1]. Therefore, the CG topology is adopted in this work. To further enhance the input matching bandwidth, a cascaded L-type input matching network (IMN) is proposed, which is composed of two single L-type networks cascaded in series. Compared with traditional T-type, Pi-type and single L-type networks [2], a cascaded L-type network can achieve the widest bandwidth [3]. Although the noise figure of a CG LNA is higher than that of a CS LNA, some circuit structures can be employed to reduce it. In this work, the current-reused structure is adopted to reduce power consumption. And it is also beneficial to the high gain and low noise design. Furthermore, a high-value resistor is laid between the MOSFET body and the ground to avoid the signal leakage and noise coupling.

To achieve high linearity, several techniques are proposed to improve the third-order input intercept point ($IIP_3$) of RF amplifiers. One example is the series feedback using source degeneration by a resistor or an inductor, and another example is the parallel feedback [4,5]. Although these methods are effective in enhancing $IIP_3$, they have drawbacks in gain reduction. Therefore, multiple gated transistor method (MGTR) is proposed by Ref. [21] as a better linearization method, which focuses on minimizing the third-order nonlinear coefficient $g_m''$ by superposing several CS transistors with given biases and widths in parallel [21]. The traditional MGTR is often used for small signal linearization scheme, and applied to the first stage in the chain [6,20]. But when it is used in the last stage, the effectiveness of the traditional MGTR is restricted. Because as the input signal increases, the transconductance $g_m$ is not constant versus the input amplitude, which limits the improvement of both $IIP_3$ and $P_{in\text{-}1dB}$ (input 1 dB compression point). Therefore, when the input signal is large, it is not enough to improve linearity by only minimizing the coefficient $g_m''$. In this work, considering the linearity of the proposed LNA largely depends on the last stage, the optimized MGTR is proposed and

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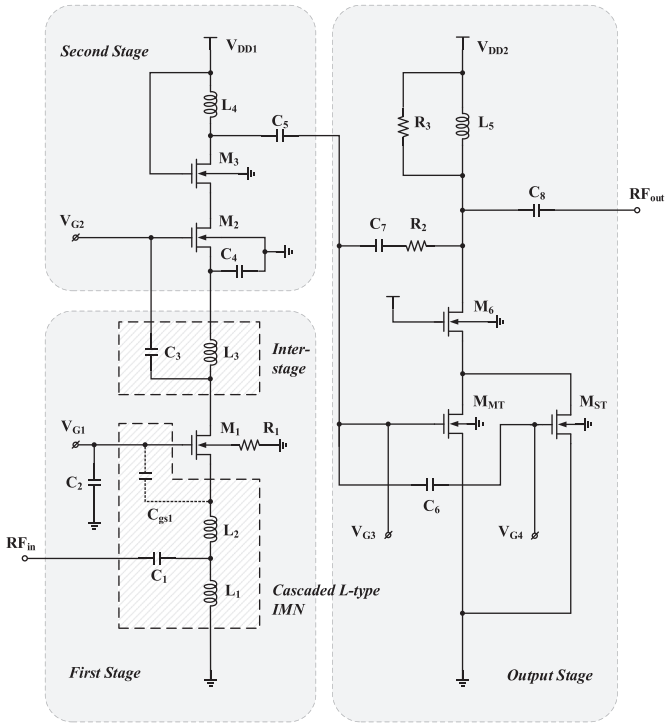


**Fig. 1.** Schematic of the proposed LNA.

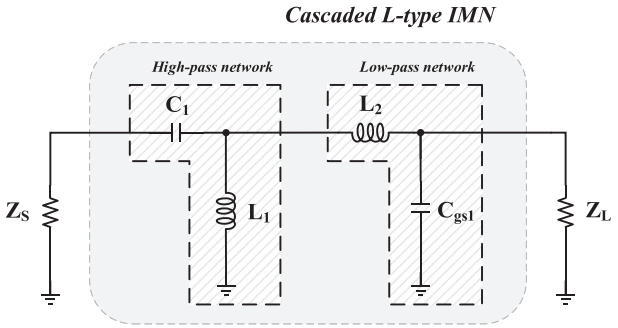


**Fig. 2.** Equivalent circuit of the cascaded L-type IMN.

applied to the output stage. The proposed optimized MGTR takes both transconductance $g_m$ and coefficient $g''_m$ into consideration when the input signal is large. It uses the secondary transistor (ST) biased in sub-threshold regime to compensate for both $g_m$ and $g''_m$ of the main transistor (MT), which has little effect on power dissipation and gain reduction. Since the voltage gains of the first two stages are high enough, the noise caused by the secondary transistor (ST) can be neglected.

In this paper, a 2–3 GHz current-reused LNA is proposed and realized for the first time utilizing cascaded L-type IMN and optimized MGTR. Based on these techniques, a wideband LNA is implemented by standard 0.18-$\mu$m CMOS technology, which demonstrates a minimum NF as low as 3.1 dB and an input matching across 1.8–5.8 GHz with a high power gain of 28.0 dB and a high $IIP_3$ of −9.89 dBm while consuming only 6.49 mA from a 3 V power supply.

## 2. Circuit topology and analysis

Fig. 1 shows the schematic of the proposed LNA utilizing the current-reused technique, cascaded L-type IMN and optimized MGTR. As can be seen, the proposed LNA can be regarded as a three-stage cascaded amplifier. The first stage is a CG amplifier ($M_1$), the second stage is a cascode amplifier ($M_2$ and $M_3$), and the output stage is a cascode

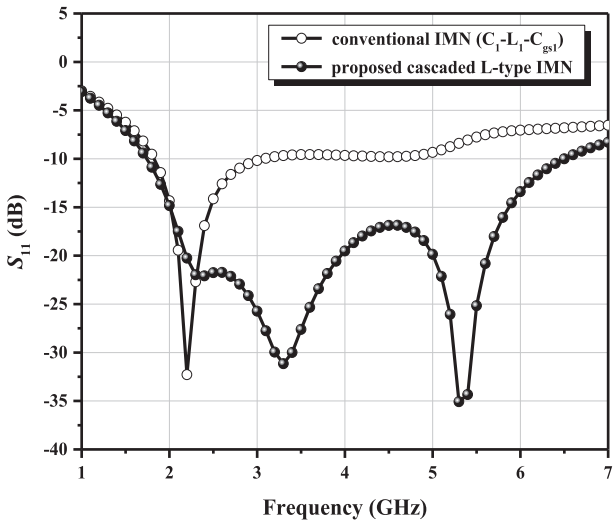


**Fig. 3.** Simulated $S_{11}$ versus frequency characteristics.

amplifier ($M_{MT}$, $M_{ST}$ and $M_6$) with a conventional resistive feedback structure.

The proposed LNA is designed for a radar system, whose supply voltage is set as 3 V. Therefore, a supply voltage of 3 V had to be used in the proposed LNA for compatibility. The three superposed transistors ($M_1$, $M_2$ and $M_3$) and the two transistors in parallel ($M_{MT}$ and $M_{ST}$) utilize 1.8 V MOSFETs, while the cascode CG transistor ($M_6$) in the output stage utilize a 3.3 V MOSFET, so that all transistors can be guaranteed operating safely under this high supply voltage.

In the first stage, the CG topology and cascaded L-type IMN are utilized to enhance the input matching bandwidth. The cascaded L-type IMN is composed of the high-pass network ($L_1$ and $C_1$) followed by the low-pass network ($L_2$ and $C_{gs1}$ (gate-source parasitic capacitor of $M_1$)). In the second stage, the cascode topology is used to increase the voltage gain and make a good isolation. By inserting the inter-stage network ($L_3$ and $C_3$), the current-reused technique is employed in the first two stages, so the bias current is shared and the power dissipation is reduced. In the output stage, the optimized MGTR composed of $M_{MT}$ and $M_{ST}$ is used to enhance the linearity of the whole circuit. And the cascode feedback (resistive feedback structure $R_2$ and $C_7$) is adopted to achieve wideband output matching [23,24].

### 2.1. Cascaded L-type input matching network (IMN)

In the proposed LNA, the cascaded L-type network is utilized as the IMN. As shown in Fig. 2, the equivalent circuit of the cascaded L-type IMN is composed of two single L-type networks cascaded in series (the high-pass network followed by the low-pass network). $Z_S$ is the input source resistance of 50 Ω, and $Z_L$ is the equivalent resistance seen at the source of the $M_1$ in Fig. 1, which equals to 90 Ω obtained by simulation.

At high frequencies (HF), the high-pass network gives a low impedance path for RF signal, then the load resistance $Z_L$ can be matched to the source resistance $Z_S$ by the low-pass network. Therefore, there is a dip in $S_{11}$ at frequency around

$$f_{HF} = \frac{1}{2\pi}\sqrt{\frac{1}{Z_L^2 C_{gs1}^2} - \frac{1}{L_2 C_{gs1}}}, \tag{1}$$

Similarly, at low frequencies (LF), the low-pass network gives a low impedance path for RF signal, then the load resistance $Z_L$ can be matched to the source resistance $Z_S$ by the high-pass network. Therefore, there is another dip in $S_{11}$ at frequency around