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A high accuracy voltage reference generator

George Souliotis [a,*], Fotis Plessas [b], Spyridon Vlassis [c]

[a] Department of Electrical Engineering, Technological Educational Institute of Western Greece, Patras, Greece
[b] Department of Electrical and Computer Engineering, University of Thessaly, Volos, Greece
[c] Electronics Laboratory, Department of Physics, University of Patras, Patras, Greece

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ABSTRACT

A high-accuracy voltage reference generator is proposed in this paper. It has been designed in a CMOS 65 nm technology node, operating with a typical supply voltage of 1.2 V, which provides a reference voltage equal to 0.5 V. Measurement results of the fabricated chip show a reference voltage variation less than 0.04% over temperature range from −40 to 125 °C and less than 0.9% over temperature and supply voltage corners. The proposed design demonstrates a low noise output and good performance under mismatch. A current reference generator has been included in the design to provide a constant reference current. The measured variation of the reference current is about 1%.

1. Introduction

Analogue circuits are used in many electronic devices for several applications, such as communications, biomedical electronics, portable devices, computer systems and others. Analogue circuits however, are sensitive in variations of the supply voltage, the bias current, the temperature and the fabrication process. To reduce their sensitivity, a constant voltage reference or a constant current reference is required to bias the analogue circuits. A voltage reference generator produces a constant voltage independent of the temperature and supply voltage [1]. Implementations of voltage reference generators, known as Bandgap Voltage Reference (BGR) Generators, usually, were designed to generate a constant voltage around 1.26 V at 27 °C (300 K). This value is compatible with the silicon bandgap value [2,3] and it is suitable for BJT based circuits. Also, the reference voltage of 1.27 V was used in the first generation of MOS based circuits operating with higher threshold and supply voltage comparing with the modern circuits. As the constant reference voltage was 1.26 V the required supply voltage was greater than 1.4 V in order to achieve reasonable power supply rejection ratio (PSRR). However nowadays, these values of the supply and the reference voltages are too high for the recent circuits designed for portable devices, which must operate with much lower supply voltage. Therefore, the most recent voltage reference generators, not only operate under lower supply voltage but also, they generate lower reference voltage, as well. A typical value for the reference voltage is around 0.5 V, close to the threshold voltage of an NMOS transistor.

Several topologies have been proposed for voltage reference generators. BiCMOS topologies were introduced in Refs. [4–6], however they are rarely used in modern systems due to the high power consumption. Other CMOS based voltage generators -adopt special design techniques, such as the dynamic threshold MOS transistors (DTMOST) used in Ref. [7]. In this, the transistors must be designed with separated wells making the layout design large, prone to mismatches and requiring triple well CMOS technology nodes. In Ref. [8], the proposed sub-1V voltage reference generator uses native transistors, which require an extra mask and therefore the fabrication process is more expensive. In addition, the employment of native transistors may limit the porting ability to other technology nodes. Furthermore, in Ref. [8], the required operational amplifiers (OAs) operate with 2.1 V and thus, the advantage of the sub-1V operation is totally vanished. The circuit reports operation from 0 to 125 °C.

Some 1 V topologies are designed based on transistors operating in weak inversion region to reduce power consumption and to avoid the employment of bipolar PNP devices [9–20]. These topologies, although dissipate low power however, they offer operation in a relatively small temperature range, in some cases up to only 80 °C. In Refs. [21] and [22], low voltage, low power, topologies based on weak inversion operation are reported. An internal, VDD charge-pump doubler and a clocked switched-capacitor V_{BE} divider are used. Thus, a buffer is needed to drive high load currents, increasing the total power consumption. Reference voltage generators based on weak-inversion transistor are more sensitive in voltage variations or they are prone to instability requiring large

* Corresponding author.
E-mail addresses: gsoul@teiwest.gr (G. Souliotis), fplessas@e-ce.uth.gr (F. Plessas), svlassis@physics.upatras.gr (S. Vlassis).

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capacitors for compensation [23,24]. They may be suitable for extremely low power consumption systems, but they may not be suitable when the generated reference voltage drives a large load. Furthermore, most of them operate in relatively low temperature range. Topologies based on CMOS only transistors, with extended temperature range compared to others, are presented in Refs. [25,26]. Circuits based on more conventional topologies are proposed in Refs. [27–29]. Some of the topologies require high gain [24] or rail-to-rail operational amplifiers [28], which makes the design more complicated. A review for voltage reference generators takes place in Ref. [30] and start up considerations are studied in Ref. [31]. A study of the effect on the circuit operation under temperature variations is given in Ref. [32]. The most important property of the voltage references generators is the low dependency of the reference voltage under process, voltage and temperature (PVT) variations. Two other important properties are the stability and the driving capability.

A voltage reference generator is proposed in this paper, based on the two operational amplifiers topology presented in Ref. [28]. The architecture has been optimized through a detailed theoretical analysis in terms of performance, silicon area, and power consumption. Compared with [28], the proposed circuit does not employ rail-to-rail operational amplifiers, and thus, it is simpler in design and more compact in layout. The bias current of the operational amplifiers is properly selected to reduce the final output voltage variations. The proposed design does not require any external large capacitor for filtering or stability and this is an important improvement. During the theoretical analysis, small resistors have been chosen, making the layout significantly smaller compared with [28]. A current reference generator has been employed together with the voltage reference generator whereas the noise performance is also examined. Finally, the work from Ref. [28] reports only simulation results while we demonstrate the efficiency of the optimized architecture by implementing and validating it. Measurement results show very good agreement with simulation results, significant improvement in the performance compared to [28], and the effectiveness and robustness compared to other recent designs. In Sections 2 and 3 the proposed topology is studied and in Section 4, measurement and simulation results of the fabricated chip are provided. The conclusions are given in Section 5.

2. Circuit analysis of the proposed BGR

The electrical behavior of the semiconductor elements is significantly affected by the wide temperature variation. When a constant voltage is required, it can be generated by combing an electrical quantity with positive temperature coefficient (TC) with an electrical quantity with negative TC, as shown in Fig. 1. The first gives a Proportional-To-Absolute-Temperature (PTAT) quantity and the second a Complementary-To-Absolute-Temperature (CTAT) quantity.

The base-emitter voltage V_{BE} of a bipolar transistor has a negative TC about -2 mV/°C and the thermal voltage V_T has a positive TC of 0.085 mV/°C. Assuming that $V_{BE} \gg V_T$, the operation of the transistor is given by the known approximate equation,

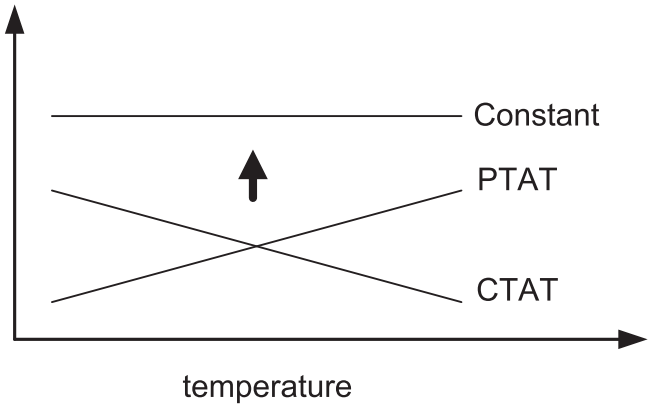

Fig. 1. Constant voltage generation by a PTAT and a CTAT voltage.

$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \tag{1}$$

where, I_S is the reverse saturation current, $V_T = kT/q$, k is the Boltzmann constant, T is the absolute temperature and q is the electrical charge of an electron.

The topology of the BGR is shown in Fig. 2. The Operational Amplifier (opamp) OA1 biases properly the PMOS transistors M_1 and M_2 in order that,

$$V_A = V_B \tag{2}$$

The voltages V_A and V_B are,

$$V_A = I_1 \cdot R_1 + V_{BE1} \tag{3}$$

$$V_B = V_{BE2} \tag{4}$$

The emitter area of the transistor Q_1 is N times greater than that of Q_2. Then from (1),

$$V_{BE1} = V_T \cdot \ln(I_1/N \cdot I_S) \tag{5}$$

$$V_{BE2} = V_T \cdot \ln(I_2/I_S) \tag{6}$$

As the transistors M_1 and M_2 are biased by the same gate-source voltage, they create the same drain current and therefore, $I_2 = I_1$. The difference of V_{BE} for the same current of the two bipolar transistors can be found by (5) and (6) as,

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \cdot \ln(N) \Rightarrow \Delta V_{BE} = \frac{\ln(N) \cdot k \cdot T}{q} \tag{7}$$

From (2)–(4),

$$I_1 = \frac{V_T \cdot \left(\ln\left(\frac{I_2}{I_S}\right) - \ln\left(\frac{I_1}{N \cdot I_S}\right) \right)}{R_1} \tag{8}$$

or

$$I_1 = \frac{V_T \cdot \ln(N)}{R_1} \tag{9}$$

So, I_1 ($= I_2$) is a PTAT current, proportional to ΔV_{BE} and it is created by transistors M_1, M_2 and M_3. Especially M_3 makes a copy of I_1 at the output node V_{ref}. It is obvious that the PTAT current depends on the transistors' area ratio N of Q_1 and Q_2. The resistor R_1 generates the difference in the emitter-base voltage between the two BJTs Q_1 and Q_2. The CTAT current is generated by OA2 and M_4. The current I_3 is suitably set in order that,

$$V_C = V_B \tag{10}$$

Since $V_B = V_A$,

$$V_C = I_1 \cdot R_1 + V_{BE1} = V_{BE2} = I_3 \cdot R_2 \tag{11}$$

From eq. (11) it is shown that $I_3 = V_{BE2}/R_2$ and as V_{BE} is CTAT then I_3 is CTAT. From (11) and (9),

$$I_3 = \frac{V_T \cdot \ln(N)}{R_2} + \frac{V_{BE1}}{R_2} \tag{12}$$

Considering that V_C must be close to V_B and V_A, without however the existence of a V_{BE} voltage, and for keeping R_2 at low value for a small layout, I_3 must be greater than I_1 by a factor of K. Summing proportionally the currents I_1 and I_3 a constant current is produced. However, the two currents are not equal and a gain factor must be applied to I_1. The total current must be temperature independent, meaning that,