Microelectronics Journal 75 (2018) 75–86

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Energy efficient design of CNFET-based multi-digit ternary adders

Chetan Vudadha [a,*], Sai Phaneendra Parlapalli [a], M.B. Srinivas [b]

[a] BITS-Pilani, Hyderabad Campus, Hyderabad, India
[b] School of Engineering and Technology, BML Munjal University, Gurgoan, India

ARTICLE INFO

2010 MSC:
00–01
99-00

Keywords:
CNFET
Multi-digit adders
Ternary logic
Low power

ABSTRACT

This paper proposes a new technique to implement multi-digit ternary ripple-carry adders in Carbon-nanotube field effect transistor (CNFET) Technology. The proposed multi-digit adder uses efficient half-adders to generate Half-Sum (*HS*) and Half-Carry (*HC*). These half-adder outputs (instead of main inputs) are used to compute carry-out at each digit-adder stage using a delay optimized carry generator. The half-sum and carry-out are then used to compute final sum at each digit-adder stage with the help of a sum generator and low-power encoders. Employing delay optimized carry generator along with low-power encoder results in energy efficient multi-digit ternary adder design. Existing and the proposed multi-digit adders of varied operand sizes are implemented in HSPICE. Simulation results show that the proposed multi-digit adder designs result in up to 52% reduction in average power consumption and 58% reduction in Power-Delay Product (PDP), when compared to other multi-digit adders in the literature.

1. Introduction

Traditionally, digital computation is performed on two-valued logic, also called binary logic. However, Multi-Valued Logic (MVL), has received considerable attention due to energy efficiency of the circuits resulting from reduced complexity of interconnects and chip area. Ternary logic [1] is a special case of MVL where computation is performed on three-valued logic. Ternary logic circuit design using CMOS can be found in literature [2,3]. MOSFET-based implementation of a 2-bit ternary ALU (T-ALU) slice is presented in Ref. [4]. It has been shown that the performance of CMOS-based designs can be enhanced by adding MVL blocks to binary designs [5]. There are two kinds of MVL circuits which are based on MOS technology. One is current mode MVL circuit and the other is voltage mode MVL circuit. Voltage mode MVL is achieved by multi-threshold CMOS design [6]. Implementation of multiple threshold values in CMOS is complex and can be achieved by using different bias voltages to the bulk terminal of the transistors.

Carbon-Nanotube (CNT) field effect transistor (CNFET) is a promising alternative to MOS transistor to achieve high performance at low power consumption in logic circuit design [7,8]. CNFETs use single walled CNT as a conducting channel, which can be conducting or semiconducting depending on the angle of atom arrangement along the tube, also called as chirality vector. The threshold voltage of CNFETs depends on the diameter of the CNT which in turn depends on the chirality vector. This dependence makes CNFET suitable for implementation of MVL circuits. Apart from conventional CNFET, new types of CNFET like gate-all-around (GAA) CNFET [9], which provides the conditions for scaling the technology to 10 nm and beyond, are also being explored. While interest in design of CNFET-based logic circuits waned over recent years due to complex fabrication technology and reliability issues, recent demonstration of a CNFET-based processor/computer by Stanford researchers [10] has reignited this interest.

CNFET-based ternary logic circuits using resistive loads have been presented in Ref. [11]. The disadvantage of this approach however is that it needs large off-chip resistances. A more efficient design methodology, which eliminates the need for large resistances by employing an active load with P-type CNFETs, has been presented in Refs. [12,13]. Another CNFET-based design methodology, which uses pseudo N-type CNFETs, has been presented in Ref. [14]. Recently there have been many implementations of CNFET-based ternary arithmetic circuits (like Comparator [15], Adders [16–25] and ALU [26]) that focus on optimizing the design parameters. Recently a serial adder, which uses a 1-bit ternary adder and a ternary D flip-flop, has been proposed in Ref. [27]. Apart from arithmetic circuits, implementations of sequential elements like Schmitt Trigger-Based latch [28], D flip-flop [27] etc. can be found in the literature. In this paper we propose a multi-digit ternary adder that uses an efficient half-adder, a delay optimized carry generator, a

* Corresponding author.
E-mail address: chetan@hyderabad.bits-pilani.ac.in (C. Vudadha).

https://doi.org/10.1016/j.mejo.2018.02.004
Received 21 September 2017; Received in revised form 8 February 2018; Accepted 21 February 2018
Available online XXX
0026-2692/

sum generator and low-power encoders. Each of the blocks is optimized for delay and power consumption.

Rest of the paper is organized as follows: Section 2 presents the background for ternary logic and CNFETs. A brief overview of the existing work related to CNFET-based ternary adder design is presented in Section 3. The proposed technique to implement the multi-digit ternary adders is presented in Section 4. This section also presents new designs for blocks such as decoder, carry generator etc, that are used in the implementation of the ternary adders. Simulation results are presented in Section 5 while conclusions are drawn in Section 6.

2. Background

2.1. Review of ternary logic

The binary logic when given a significant third value is called ternary logic or three valued logic and functions realized with three values are called ternary logic functions. The values 0, 1 and 2 form the nomenclature to denote the ternary values in this paper. A function $f(X)$ is defined as a ternary logic function mapping $\{0,1,2\}^n$ to $\{0,1,2\}$ where X is given by $X_1, \ldots, X_n$. When $X_i, X_j \epsilon \{0,1,2\}$, the basic operations of ternary logic can be defined as:

$$X_i + X_j = \max\{X_i, X_j\} \tag{1}$$

$$X_i \cdot X_j = \min\{X_i, X_j\} \tag{2}$$

where equations (1) and (2) indicate OR and AND operations respectively for ternary logic [13]. Another important logic function in ternary logic is a ternary inverter. Table 1 shows the outputs of different ternary inverters that are used in ternary logic. Corresponding to each of the outputs three inverters are defined namely, Negative Ternary Inverter (NTI), Standard Ternary Inverter (STI) and Positive Ternary Inverter (PTI) respectively. The logic values assumed for different voltage levels are shown in Table 2 where, voltages 0, $Vdd/2$ and Vdd correspond to logic values 0, 1 and 2 respectively.

Implementation of ternary logic circuits require transistors with different threshold voltages. Hence CNFET technology, where the threshold voltage of transistor can be modified by changing its physical dimensions, is suitable to implement ternary logic circuits [13]. The following section presents a brief overview of CNFET.

2.2. Carbon nanotube field effect transistor (CNTFET)

CNFET is a promising alternative to MOSFET for achieving low power and high performance. CNFETs use a semiconducting single walled CNTs as a channel for conduction. The angle of atom arrangement along the tube in a single wall CNT (SWCNT) makes it either conducting or semiconducting. This unique property of the SWCNT is referred to as the chirality vector and is represented by an integer pair (n,m), called the indexes which determine if the CNT is metallic or semiconducting. The nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer, otherwise it is semiconducting. The chirality vector also sets the diameter of the CNT that determines the drain current through the CNFET. The drain current is directly proportional to the number of CNTs connected between source and the drain and their respective diameters [29,30].

The threshold voltage of the CNFET is inversely proportional to the diameter of CNT which, as mentioned above, depends on its chirality vector. It is the threshold voltage controllability of CNFET that makes it well suited for the implementation of multi-valued logic circuits. The relationship between chirality, CNT diameter and threshold voltage can be derived from relations presented in Ref. [29] and is shown in Table 3. While techniques exist to synthesize CNFETs of desired chirality [31,32], those with three chiralities i.e. $(19,0)$, $(13,0)$ and $(10,0)$ are normally used in the implementation of CNFET-based ternary logic circuits [13].

Table 1
Ternary Inverters [13].

Input x	NTI (x)	STI (x)	PTI (x)
0	2	2	2
1	0	1	2
2	0	0	0

Table 2
Logic symbols.

Voltage Level	Logic Value
0	0
$Vdd/2$	1
Vdd	2

3. Related work

Adder is the basic building block of Arithmetic and Logical Unit (ALU), which in turn is an integral part of any general purpose processor. Adders are also used in many hardware implementations like logarithmic converters, address generators etc. There have been many CNFET-based ternary adder designs proposed in the literature. A brief overview of these adders is presented in the following subsections.

3.1. Single-digit adders

The ternary adder presented in Ref. [13] uses a ternary decoder in the first stage to generate binary versions of inputs. The ternary decoder is a one-input, three-output circuit and generates unary functions for an input X. The relation between ternary input X and decoder outputs (indicated by X^0, X^1, X^2) is given by

$$X^k = \begin{cases} 2, & if \quad X = k \\ 0, & if \quad X \neq k \end{cases} \tag{3}$$

or alternatively

$$X^0 = \begin{cases} 2 & if \quad X = 0 \\ 0 & if \quad X = 1,2 \end{cases}$$

$$X^1 = \begin{cases} 2 & if \quad X = 1 \\ 0 & if \quad X = 0,2 \end{cases}$$

$$X^2 = \begin{cases} 2 & if \quad X = 2 \\ 0 & if \quad X = 0,1 \end{cases}$$

These decoder outputs can take only two logic values i.e., *logic* 2 and *logic* 0, corresponding to *logic* 1 and *logic* 0 in binary logic. The decoder outputs are used to compute intermediate binary outputs with the help of binary logic gates. Finally ternary sum and carry are generated from

Table 3
Relation between chirality, CNT diameter and threshold voltage [29].

Chirality	Diameter of CNT	Threshold Voltage of N-CNTFET	Threshold Voltage of P-CNTFET
$(19,0)$	1.487 nm	0.289 V	−0.289 V
$(17,0)$	1.330 nm	0.328 V	−0.328 V
$(16,0)$	1.253 nm	0.348 V	−0.348 V
$(14,0)$	1.100 nm	0.398 V	−0.398 V
$(13,0)$	1.018 nm	0.428 V	−0.428 V
$(11,0)$	0.861 nm	0.506 V	−0.506 V
$(10,0)$	0.783 nm	0.559 V	−0.559 V