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Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology

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ABSTRACT

The simple square-law MOSFET model fails to describe the behavior of short channel and moderate/weak inversion devices. The gm/ID methodology is a promising technique that addresses the square-law shortcomings and bridges the gap between hand analysis and simulation. This paper describes a systematic procedure for the design of a single-stage operational-transconductance amplifier (OTA) using the gm/ID methodology. Both small signal and large signal specifications are used to constrain the design process, which is graphically illustrated using trade-off charts. The presented design procedure is automated using MATLAB, and an iterative procedure is used to take the OTA self-loading into consideration. Moreover, an automated optimization procedure is presented to maximize the speed of a unity-gain buffer under current consumption, DC gain, and input capacitance constraints. The designed circuits are verified using Cadence Spectre and the 180 nm Predictive Technology Model (PTM), where the simulation results are in close agreement with hand analysis and automation results.

1. Introduction

Analog IC design will always be there because we live in an analog world. Analog-to-digital converters (ADCs) and digital-to-analog converter (DACs) will always be needed (together with their associated circuits such as amplifiers, filters, references, and regulators) to interface between our analog world and our digital electronic devices. It may be thought that CMOS analog design is an art that depends on lots of experience and intuition. One reason that may support this claim is that the simple square-law MOSFET model common to most textbooks and university courses fails to describe the behavior of short channel devices, as well as devices operated in moderate and weak inversion (which are becoming increasingly popular in energy-efficient designs [1–3]) regardless of their channel length. On the other hand, more accurate device models are too complicated, and are not amenable to hand analysis. In addition, there is no definite systematic recipe that the designer can follow to design an analog block, even if it is a fundamental block like an operational transconductance amplifier (OTA). As a result, the analog designer has to rely on lengthy multi-variable sweeps on simulation tools, experience, and intuition to make his design work. In addition to requiring significant design time and expensive simulation tools licenses, this design methodology hinders the understanding of design trade-offs, the development of valuable designer intuition, and the systematic porting of designs from one technology node to another.

A promising methodology that addresses the previous limitations, and bridges the gap between hand analysis and simulation is the g_m/I_D design methodology [4–9]. The basic idea of this methodology is to describe the transistor behavior using a dataset generated from simulation sweeps (or measurements) rather than inaccurate simple models. This dataset characterizes different normalized transistor parameters and figures-of-merit vs the transconductance-to-current ratio (g_m/I_D). The g_m/I_D is used as a primary design variable instead of the overdrive voltage which is common in square-law based design flow. The g_m/I_D can be thought as a normalized measure of the channel inversion level for all operating regions, and it directly captures the relation between the basic function of the transistor (the transconductance) and the most valuable resource (the power consumption). The g_m/I_D dataset is one-time generated for a given technology, and can be reused in the form of trade-off charts or lookup tables. The design process becomes a systematic procedure, where hand analysis expectations are in close agreement with simulation results.

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One of the early works that discussed the g_m/I_D methodology was proposed by Silveira et al. in Ref. [4]. This pioneering work proposed using the g_m/I_D methodology for OTA design; however, several design variables were assumed without being constrained by clear circuit specifications. In addition, the details of the optimization procedure used to select the g_m/I_D values and the transistor sizing were not explained. Moreover, important circuit specifications such as input range, noise, and common-mode rejection were not considered. Finally, it did not consider the variation of the g_m/I_D characteristics with channel length, since this variation was negligible for the 3 μm technology used in the design. The g_m/I_D methodology was used to optimize a gain boosted cascode in Ref. [5]. However, similar to [4], it suffered from the same previously mentioned drawbacks. The optimization of a three-stage nested-Miller OTA using g_m/I_D methodology was proposed in Ref. [8]. The design procedure aimed at optimizing both noise and settling time specifications. However, it neglected other circuit specifications, and assumed that the g_m/I_D values and channel lengths of all transistors are known a priori. A common shortcoming in the aforementioned works is that they do not demonstrate a fully-constrained complete design example. Lastly, it is difficult for the interested designer to replicate or apply the proposed design procedures due to the lack of details and the use of proprietary device models.

As a result, there is a need for a complete and detailed design example that clearly demonstrates the g_m/I_D methodology for a simple but real-life analog block, starting from a complete set of specifications and up to verification. This paper aims at providing such a design example to promote the g_m/I_D methodology among experienced designers who are not used to this powerful methodology, as well as novice designers who are embarking their analog IC design journey. A key merit that differentiates this work is that it clearly explains the design and optimization procedure for a complete design example using publicly available device models. Consequently, the interested reader can replicate the results, or apply the presented techniques to his own design problems. A simple single-stage OTA (also known as five-transistor OTA [10]) is used as a design example, which despite its simplicity still finds use in complex mixed-signal systems (e.g. [11]). The OTA design process is constrained by both small-signal and large-signal specifications, and is graphically illustrated using trade-off charts. The presented procedure is automated using MATLAB, and the automation program is applied to solve more sophisticated design problems. Analytical expressions for the OTA self-loading and input capacitance are derived, verified, and used in the automation program. The proposed design examples are verified using Cadence Spectre and the publicly available 180 nm Predictive Technology Model (PTM) [12].

2. Systematic design procedure using g_m/I_D trade-off charts

2.1. OTA specifications

The target design example is a single-ended output five-transistor OTA to be used as a unity-gain buffer to drive a large capacitive load. The design specifications are shown in Table 1. The available current consumption for the OTA is 20 μA. In addition, a 10 μA reference current is externally provided. The OTA gain-bandwidth product (GBW) is roughly equal to the buffer closed-loop bandwidth (BW_{CL}), and the OTA common-mode input range (CMIR) is itself the buffer input range.

2.2. Trade-off charts generation

DC simulation is used to generate the operating point parameters, and AC noise simulation is used to extract the value of the noise coefficient (γ). DC sweep is used for V_{GS} from $\approx V_{TH} - 100$ mV to $\approx V_{TH} + 500$ mV. Parametric sweep is used for the channel length (L). The channel width (W) is kept constant since the transistor parameters are approximately proportional to W regardless of the operating region. A channel width of 10 μm is selected to avoid narrow width effects, not-

Table 1
OTA specifications.

Technology	0.18 μm CMOS
Supply Voltage	1.8 V
Reference Current	10 μA
Current Consumption	20 μA
Capacitive Load	5 pF
Gain-Bandwidth Product	5 MHz
Phase Margin	70°
Open-Loop DC gain	32 dB
Total Integrated Thermal Noise	50 μVrms
Input Range	0.2 V – 1.1 V
Common Mode Rejection Ratio (CMRR) @ DC	70 dB

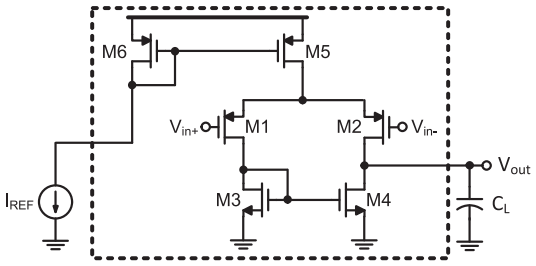

Fig. 1. Schematic of the five-transistor (5 T) OTA. I_{REF} and C_L are external elements used in the testbench. The feedback connection for unity-gain buffer operation is not shown.

ing that relatively large W is typically used for analog circuits. A finger width of 2 μm is assumed; thus, all widths are selected to be multiples of 2 μm. Since three transistors are stacked in the targeted OTA architecture, V_{DS} is set at $V_{DD}/3$. The previous simulations are performed only once, and the results can be saved in the form of charts or lookup tables for further reuse.

2.3. Design of the input pair

The first step is to choose the type of the OTA input pair. Since the required input range (0.2 V – 1.1 V) is close to the ground rail, a PMOS input stage is necessary. The schematic of the OTA is shown in Fig. 1. From the GBW and C_L specifications the transconductance of the input pair can be determined [10].

$$GBW = \frac{g_{m1,2}}{2\pi C_L} \tag{1}$$

where the OTA internal capacitors were neglected compared to the large output load (more about this point in Section 2.6 and Section 3). Substituting in (1) yields $g_{m1,2} \approx 160$ μS. Since the 20 μA OTA bias current is split equally between M1 and M2, the g_m/I_D of the input pair is

$$(g_m/I_D)_{1,2} \approx 16\ S/A \tag{2}$$

The channel length can selected from the gain spec. The differential DC gain of the OTA is given by Ref. [10].

$$A_{vdc} = \frac{g_{m1,2}}{g_{ds2} + g_{ds4}} \tag{3}$$

From (2) and Table 1, the requirement on the output conductance of M2 and M4 is

$$g_{ds2} + g_{ds4} < 4\ \mu S \tag{4}$$

It is fair to assume that this requirement is split equally between M2 and M4, i.e., M2 and M4 have the same output conductance ($g_{ds2} = g_{ds4} <$ 2 μS). Thus, the intrinsic gain of the input pair is constrained by

$$(g_m/g_{ds})_{1,2} \geq 80 \tag{5}$$