Microelectronics Journal 74 (2018) 49–59

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder

Majid Amini-Valashani, Mehdi Ayat, Sattar Mirzakuchaki *

Department of Electrical Engineering, Iran University of Science and Technology (IUST), Tehran, Iran

ARTICLE INFO

Keywords:
Arithmetic
XOR-XNOR cell
Full adder
Hybrid design scheme
Low-power

ABSTRACT

A novel full-swing, low-power and energy-aware full adder using hybrid logic scheme is presented in this paper. At first, a new energy-efficient 10T XOR-XNOR cell is designed by modifying inverter and pass transistor based 3T XOR-XNOR gates combined with a feedback loop. The performance of this new cell is compared with some reported ones and then, using this new cell and two other modules, a novel full adder circuit is proposed and evaluated in TSMC 0.18 μm CMOS process technology. Post-layout simulations using Cadence Virtuoso tool showed 33%–74% and 35%–81% improvement in terms of power consumption and power-delay product (PDP), respectively, compared with some well-known counterparts in the literature. Furthermore, high-performance claim of our proposed full adder cell is verified through the process, voltage and temperature (PVT) variations' simulation of the adders. Finally, implementation of different full adders in 4-bit ripple carry adders (RCAs) proved our new design has high performance in the aspects of power dissipation and PDP.

1. Introduction

In recent years, due to rapid growth in portable electronic devices such as personal digital assistants (PDAs), smart phones and laptop computers, demand for low-power, high-speed and small chip area circuits has been largely investigated in VLSI circuits and systems. Arithmetic units play a vital role in all stated devices and full adder cells are the fundamental building blocks used extensively in these units. Hence, enhancing the performance features of full adders will affect the entire system performance.

Many papers have been published regarding design of full adder cells in the literature [1–9]. Although all of them carry out the same function, the internal logic structures are distinct, yielding difference in propagation delay, power consumption, size and wiring complexity of the circuits. Three main structures of reported full adder cells at module level are depicted in Fig. 1 and the logic equations are listed in Table 1, where H and $\overline{H}$ designate $A \oplus B$ and $\overline{A \oplus B}$, respectively (The logic expressions written for Fig. 1(a) are related to a special group of hybrid full adders called 'centralized full adders').

The first group of full adders are hybrid full adders which use 3-Module structure shown in Fig. 1(a) [1]. Many authors have used the best available modules or enhance them to present a power-delay efficient full adder cell based on this scheme [2,3,26]. HPSC [2] and Hybrid-CMOS [3] full adders are designed using reliable modules and provide full-swing outputs with admirable driving capability but they suffer from slow response at low voltages and high power consumption issues, respectively. Authors in Ref. [4] presented an alternative internal logic structure for the full adder cell illustrated in Fig. 1(b). They proposed two full-swing output adders based on their new architecture using double pass-transistor logic (DPL) and swing restored complementary pass-transistor logic (SR-CPL) to offer better power-delay product (PDP) value but their designs are not efficient in terms of power consumption and transistor count (28T and 26T). Fig. 1(c) shows the third internal logic approach presented by Kumar and Sharma [5]. They presented two energy-efficient 1-bit full adder cells which also occupies less area than adders in Refs. [2–4]. The most important drawback of their designs is high carry propagation delay due to sharing of input carry in two modules which causes low-speed when used in cascaded structures such as ripple carry adders (RCAs) and regular multipliers.

On the other hand, small number of transistors are adapted in designing low-power full adders such as static energy-recovery full (SERF) adder [6], 9A [7], 8T [8,9], 10T [10] and Shannon's theorem based [11] full adders. These adders occupy less area and consume less power but suffer from non-full swing outputs. As the minimum feature size of MOSFET devices is scaling down into only a few nanometers, the supply voltage should be decreased to prevent hot-carrier effects in

* Corresponding author.
E-mail address: m_kuchaki@iust.ac.ir (S. Mirzakuchaki).

https://doi.org/10.1016/j.mejo.2018.01.018
Received 5 July 2017; Received in revised form 27 November 2017; Accepted 20 January 2018

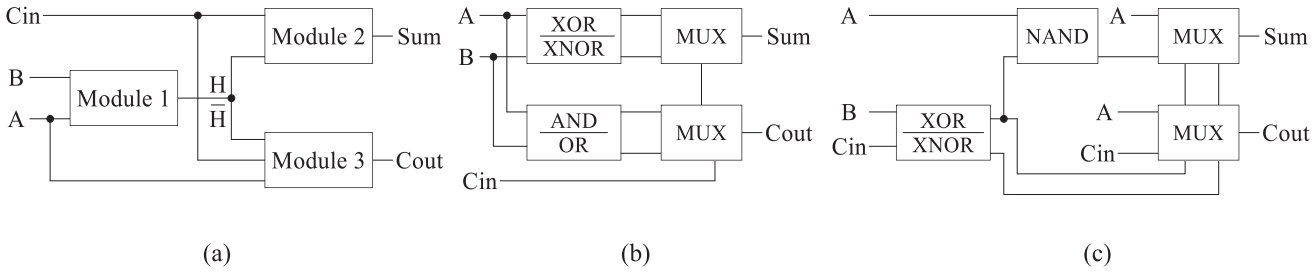

Fig. 1. Three main structures of full adder cells in the literature. (a) Hybrid design scheme [1], (b) Aguirre's logic scheme [4] and (c) Kumar's logic scheme [5].

Table 1
Logic equations of different structures shown in Fig. 1

Structure	Logic function	
	Sum	Cout
Fig. 1(a)	$H\overline{C_{in}}+\overline{H}C_{in}=(A\oplus B)\oplus C_{in}$	$HC_{in}+\overline{H}A$
Fig. 1(b)	$H\overline{C_{in}}+\overline{H}C_{in}=(A\oplus B)\oplus C_{in}$	$\overline{C_{in}}(AB)+C_{in}(A+B)$
Fig. 1(c)	$(B\oplus C_{in})\overline{(A(B\oplus C_{in}))}+A\overline{(B\oplus C_{in})}$	$A(B\oplus C_{in})+C_{in}\overline{(B\oplus C_{in})}$

CMOS circuits [12]. However, due to the mentioned problem, utilizing these adders in cascaded and bigger structures where a chain of full adders is needed may cause malfunction (especially at low voltages and submicron technologies). Consequently, an optimized design is required for full adder circuit to prevent any reduction in the output signals levels.

In this paper a new full-swing hybrid full adder cell which is more energy-efficient than previously designed ones is presented. The circuit was realized using 18 MOSFETS in TSMC 0.18 μm CMOS technology and $V_{DD}=1.8$v in Cadence Virtuoso tool and optimized to satisfy the best PDP value. Post-Layout simulations showed that power consumption (3.79 μW) and PDP (0.88 fJ) of our new design are lower compared with existing full adders. Furthermore, the design was verified to be promising by process, voltage and temperature (PVT) variations' analysis and by using it in a 4-bit RCA.

The rest of this paper is organized as follows. In section 2, a new energy-efficient circuit for Module 1 (XOR-XNOR cell) is designed. Describing possible circuits for Modules 2 and 3 and proposing a novel 18T full adder are presented in section 3. Different simulation results for both 1-bit full adders and 4-bit RCAs are reported in section 4 and section 5 concludes this work.

2. Proposed XOR-XNOR cell

2.1. Design of proposed XOR-XNOR cell

Module 1 in the structure shown in Fig. 1(a) is an XOR-XNOR cell generating H and $\overline{H}$ signals which drive some inputs of the next two modules. A variety of topologies have been proposed in the literature to realize this module using different logic styles [3,4,13–15]. In the rest of this section, we design a new high-performance XOR-XNOR circuit.

Fig. 2(a) [8] and (b) [9] show designs of XOR and XNOR gates based on modified version of Static-CMOS inverter besides a pass transistor.

These circuits use only three transistors and also don't require the complementary form of inputs but suffer from two issues. First, consider the 3T-XOR gate shown in Fig. 2(a). When input B is at high level and transistor M3 is off, the entire circuit operates like a typical inverter and complement form of input A passes to H output. But the problem occurs when input B changes to logic '0'. When $A=B=0$, the H output level equals to absolute threshold value of a pMOS transistor ($|V_{TP}|$). Authors in Ref. [8] showed that by fixing channel length of transistor M3 (L) and increasing its channel width (W), $|V_{TP}|$ can be reduced according to the threshold voltage (V_T) equation expressed below [16]:

$$V_T = V_{T0}+\gamma\left(\sqrt{V_{SB}+\varphi_0}-\sqrt{\varphi_0}\right)-\alpha_l\frac{t_{OX}}{L}(V_{SB}+\varphi_0)-\alpha_V\frac{t_{OX}}{L}V_{DS} + \alpha_W\frac{t_{OX}}{W}(V_{SB}+\varphi_0) \quad (1)$$

Where V_{T0}, γ, t_{ox}, L and W are zero bias threshold voltage, bulk threshold coefficient, oxide thickness, channel length and channel width, respectively. Also φ_0 is $2\varphi_F$ (where φ_F is Fermi potential) and α_l, α_V, and α_W are the process dependent parameters. Although increasing W/L ratio of M3 can reduce the amount of $|V_{TP}|$ and therefore, a better logic '0' is offered at H output, this output level is still unacceptable and can cause malfunction in cascaded modes and submicron technologies. The other problem occurs when $AB=10$, where transistors M1 and M3 switch *ON*. Here the output must be a perfect logic '1'. This can be achieved by passing logic '1' across transistor M3, but as transistor M1 is *ON* and tends to discharge H node to logic '0', an unknown state happens. In the case of 3T-XNOR gate shown in Fig. 2(b), when $AB=11$, the $\overline{H}$ output will be lower than normal value by V_{TN} (i.e., V_{DD} - V_{TN}) and an unknown state occurs when $AB=01$.

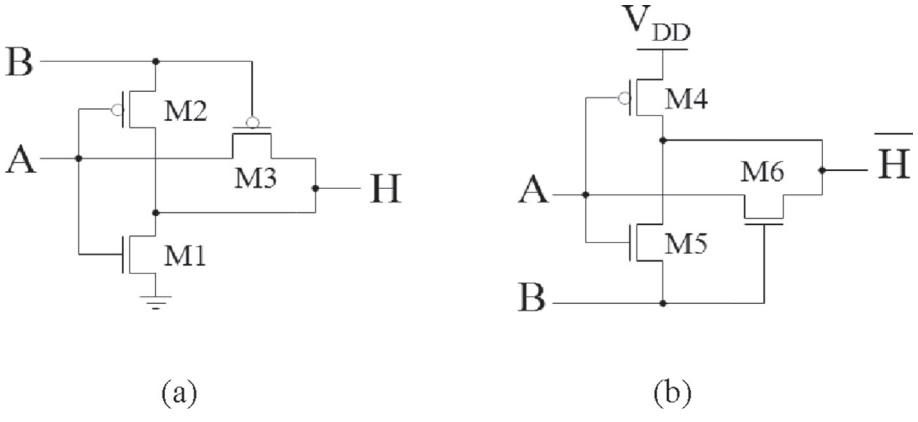

Fig. 2. XOR and XNOR gates based on inverter and pass transistor. (a) 3T-XOR gate [8], (b) 3T-XNOR gate [9].