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A high-precision time-domain RRAM state control approach

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ABSTRACT

RRAM as an analog-like element could be utilized in many interesting applications. Highly non-linear characteristics and fabrication related variations are the most important obstacles in its analog applications. To use the device in analog domain, it is required to increase the state adjustability and consider variations effects. In this paper we propose an approach, which leads to precise control of RRAM's gap length in time domain. To have a feedback of device variations a process sensor is introduced and utilized. The main idea and two proposed circuit level implementations are discussed. The applicability of the proposed method and circuits have been shown using circuit level simulations.

1. Introduction

Memristor is a device with diverse applications in both of digital and analog domains. The first well-known theory and implementation of the memristor have been reported on 1971 [1] and 2008 [2], respectively. The memristive devices include board range of state dependent emerging technologies [3]. RRAM is one of the common forms of the memristor. This device's state is a gap length, which is a function of ions position. The RRAMs are widely used in single-level [4], multi-level [5] and content addressable memories (CAM) [6]. Moreover, it is utilized as logical unit [7] and in memory as computational element [8]. It has many reported applications in analog circuits and neural networks as analog memory [9], analog computational element [10], controlling device [11] and reconfigurable factor [12]. In all these applications the RRAM's state means data or configuration.

Memristor as an analog element could be very interesting from computation perspective if it could bring back power of analog computations into conventional massively digital information process technologies. In this schema data process and storage could be combined together in a memristor-based framework. This makes it a different approach over the conventional technologies [13]. Also, RRAM as a memristor in a role of an analog device with reliable distinction between its states could cause significant improvement in data storage density [14]. Combination of multi-state memory with memristor-based analog computation could lead to an arithmetic unit which performs ordinary binary computations in completely different way.

The non-linearity and parameters variations of the RRAM [15] make its control more difficult and complicated in analog-like applications. There are previously reported approaches to use the memristor or RRAM as continues or multi-state controllable device. The cyclic phases of programming and comparison is utilized in both of analog [16,17] and digital [18] applications. The conventional iterative sequence of program and verify is relatively slow and requires lots of resources. A verify-free, direct approach has been reported [19] which is based on short pulse-trains resulting in a reliable device adjustment [19]. Controlling the current passing through the device is also frequent and conducts mostly in a 1T1R (1 Transistor 1 Resistor) configuration [20,21]. In this approach, the control mechanisms are based on gate voltage value and its time duration. There are researches which are based on ideal-memristor in flux and charge domain. They describe device state, as a function of charge or flux and so the state is controllable according to quantization of flux or charge [22].

Most of the previously proposed approaches, to utilize the RRAM in analog applications, are in time domain and because of the device non-linearity in time the controllability is very limited. To deal with the device non-linearity, we can change the design space as we proposed previously in Ref. [23], or we can try to linearize the state changes in time domain. In this paper we propose a highly-linear time-domain state controllable approach to use RRAM in analog-like applications. This approach could be utilized in multi-level memory and analog computations. First an idea is raised, which results in linear variations of RRAM's gap length in time. Then approximations and realizations are developed to have a realistic implementations. Circuit designs are considered to be as small, feasible and low power as possible. Also an RRAM variation sensor is proposed and utilized to compensate the fabrication variations. To show the efficiency of our proposed approach we introduced and used

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a Figure of Merit (FOM). To have a realistic design framework we utilized Stanford RRAM model that includes all the dynamics, temperature effects and variations inside [24]. Our design and test framework includes a standard low-cost CMOS 180 nm technology with level 49 and Verilog-A model of RRAM which could be simulate in a standard SPICE simulator. Simulation results of proposed idea and proposed circuits show that the idea could be applicable in analog applications with a good degree of confident.

The rest of the paper is organized as follows. In section 2 a brief background about memristor and RRAM is presented. The main idea will be discussed in section 3 and in sections 4 and 5 two proposed circuits are presented with their simulation results and details. In section 6 a figure of merit is introduced and employed as a comparison tool of the proposed approach. Finally, Section 7 concludes the paper.

2. Background

In this section, a brief introduction about memristor and RRAM is presented.

2.1. Memristor

Memristor is a two terminal one-port device. It describes the historically missed linkage between charge and flux. This device is a passive circuit element and named as the fourth fundamental circuit components [25]. Any two-terminal circuit component which can be expressed with equation set 1 is a memristor. In equation (1), R(x) is called memristance with unit of Ohm (Ω) and "x" is the state variable as scalar or vector. More general any resistive switching device with two property of pinched hysteresis loop and nature of shrinking the close loop area with frequency increment is a memristor [26].

$$\begin{cases} v = R(x)i \\ \dfrac{dx}{dt} = f(x,i) \end{cases} \tag{1}$$

2.2. RRAM

The physical realization of RRAM can be implemented typically in a Metal-Insulator-Metal (MIM) structure. The intensity of electric field inside the MIM structure can reach to high values (>10 MV/cm) when the thickness of insulator shrinks [27]. This electric field forces the ions inside the crystal to drift and cause state change from insulator to conductor. Historically, the properties of such phenomenon was described in 1940 [28]. The changing phase from an insulator to conductor in MIM structure has been reported in 1960s without serious target applications [29,30]. These devices with resistive switching characteristics draw more attentions when considered to be utilized in memory applications and one of the first successful reports backs to 2004 [31].

In a binary sense, RRAM could take two states of High Resistivity State (HRS) and Low Resistivity State (LRS). The processes of changing the device state from HRS to LRS is called "set" and "reset" vice versa. Furthermore, there is another process entitled "forming". The forming process performs once using higher voltage rather than normal set voltages and it is result of stress-induced defects. In this process the oxygen atoms are bring out of the lattice causing generation of defects [32]. During set and reset processes the ions inside the insulator drift toward bottom electrode (BE) and top electrode (TE), respectively. The structure and symbol of an RRAM are shown in Fig. 1 (a) and (b) respectively. This figure also shows the current direction and its effect on the gap length. Direct tunneling from cathode to anode, Schottky emission, Fowler–Nordheim (F-N) tunneling, emission from trap to conduction band, tunneling from cathode to traps, F–N-like tunneling from trap to conduction band, trap to trap tunneling, and tunneling from traps to anode, are possible conduction mechanisms [33].

2.3. Stanford RRAM model

In this paper we will used Stanford RRAM model, so we need to define the model parameters. In this model the current equation (2), is function of gap state (g) and applied voltage (V). In this equations I_0, g_0 and V_0 are the fitting parameters, where the tunneling effects considered as the main conduction mechanisms. The dynamic equation (3) by itself is function of gap state (g), applied voltage (V) and temperature (T). In equation (3), ν_0 is a velocity, includes the attempt-to-escape frequency, a is the hopping site distance, E_a is the effective activation energy, L is the device thickness, k is Boltzmann constant, q is unit electric charge, γ is the field local enhancement factor and γ_0, β, and α are all fitting parameters [24].

$$I(g,V) = I_0 \exp\left(\frac{-g}{g_0}\right)\sinh\left(\frac{V}{V_0}\right) \tag{2}$$

$$\frac{dg}{dt} = -v_0 \exp\left(\frac{-qE_a}{kT}\right)\sinh\left(\frac{\overbrace{qa(\gamma_0 - \beta g^{\alpha})}^{\gamma} V}{LkT}\right) \tag{3}$$

The ions position inside an RRAM specifies the state of the device. Applied voltage and gap state determines the electric field strait inside the device, which is responsible for ions drift. For electric field lower than a defined value (F_{min}) the ions will not drift and so the state is not changing.

3. Time-domain state control of memristor

We discussed RRAM and Stanford RRAM model in previous section. In rest of this paper RRAM and Stanford RRAM models will be used equivalently. Here we want to introduce the main idea of this paper. At the beginning let us have an observation. If a constant voltage applies over an RRAM, the gap length behavior will be as shown in Fig. 2. This figure is plotted using numerical simulations of Stanford RRAM model over time for different voltages. The gap length will remain unchanged for voltages under 1.3 v because of F_{min}. It is possible to observe that for a constant voltage, decreasing the gap length leads to increase in gap length changes speed (Δg/Δt). This behavior can be explained using plot

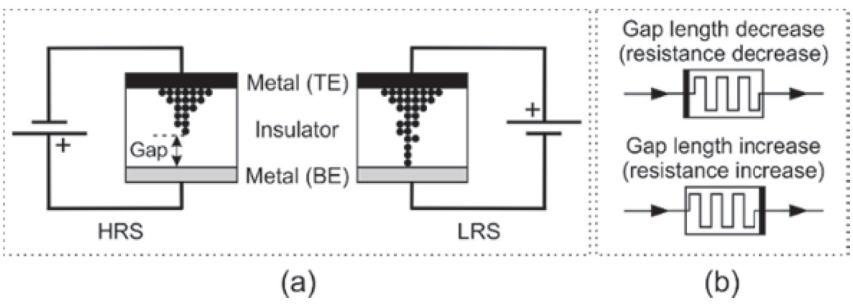

Fig. 1. RRAM structure and symbol, (a) MIM structure, (b) RRAM symbol and current direction.