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Optimization of the thermal reliability of a four-tier die-stacked SiP structure using finite element analysis and the Taguchi method

Y. Tang [a,*], S.M. Luo [a], G.Y. Li [b], Z. Yang [c], R. Chen [b], Y. Han [c], C.J. Hou [a]

[a] College of Automation, Zhongkai University of Agriculture and Engineering, Guangzhou 510225, China
[b] School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510641, China
[c] College of Engineering, South China Agricultural University, Guangzhou 510642, China

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ABSTRACT

We used finite element analysis (FEA) and the Taguchi method to investigate the reliability of a four-tier die-stacked system-in-package (SiP) structure and to achieve the optimal design of the SiP structure under thermal cycling. A finite element model of a four-tier die-stacked SiP structure was developed to simulate the thermal stress distribution in the stacked die during the thermal cycling test. Scanning electron microscopy (SEM) was used to observe the failure sites of the SiP structure. The results show that the thermal stress is concentrated in the top die and that the maximum thermal stress occurs at the outmost four corners of the bottom of the top die. A micro-crack appears in the top die, and the crack starts from the bottom of the die close to the corner of die 4. Nine geometric parameters of the SiP structure were chosen as the variable factors, and the volume-averaged maximum thermal stress $\Delta\sigma_{max}$ was chosen as the quality factor. An $L_{12}(2^9)$ orthogonal array was applied in a Taguchi experiment to estimate the effects of the nine factors and to reveal the optimal design of a four-tier die-stacked SiP structure based on the results of the thermal cycling test. The thickness of the top die has an important effect on the reliability; more than 21.2% of the volume-averaged maximum thermal stress is reduced using the optimal design.

1. Introduction

In recent years, as the requirements for small-sized portable electronic products, such as mobile phones and smartwatches, have increased, electronic components have been downsized and designed to accommodate additional functional blocks. This change has forced the packaging technology industry to shift from traditional 2-D packaging techniques to advanced 3-D stacked packaging technologies [1–3]. The system-in-package (SiP) is one of the major 3-D packaging approaches; in this approach, multiple active and passive electronic components with different functionalities are combined in a single package [4–6]. Thus, the application fields of the SiP approach are widening because of its practicality and flexibility for assembly manufacturing.

Previous work on the reliability of SiP structures has been reported. Lu et al. [7] investigated the effects of the die-shift distance of overhang dies on the residual thermal shear stress and warpage in a 5-chip stacked-die SiP and found that the maximum warpage in this assembly appears in the top left corner, with movement in the downward direction. Cheng et al. [8] used finite element analysis (FEA) to construct a 3-D TSV stacked-chip package model to investigate the thermo-mechanical behaviour of packages stressed under the temperature cycle test and noted that the most critical point for package stress is located on the bottom outermost corner of the TSV copper bump. Yu et al. [9] analysed how an embedded die affects the thermal cycling reliability of a BGA SiP and found that the failure occurs on the inner side of the BGA solder balls near the embedded die position. Kinoshita et al. [10] discussed thermal conduction and mechanical stresses in TSV structures in three-dimensional SiPs under device operation conditions. A stress concentration occurred around the void inside the TSV, and the magnitude of the equivalent stress was approximately 120 MPa. Chen et al. [11] evaluated the impact of the use of an encapsulated molding compound and underfill material on the reliability test for a low-K wire--bond-stacked flip-chip CSP and noted that a temperature cycling test stress induced delamination between the interface of the backside of the bottom die and the encapsulated molding compound. Yamada et al. [12] analysed the board-level reliability of the drop test for SiP using a simple dynamics modelling technique, showing that the maximum strain appears in a corner ball at a centre side and that the use of a thin core and a

* Corresponding author.
E-mail address: tangyu_mycauc@163.com (Y. Tang).

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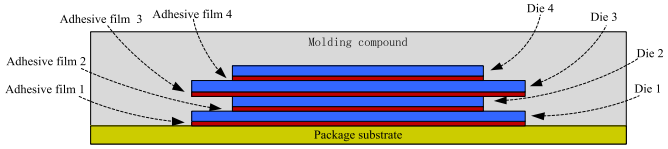

Fig. 1. Schematic of four-tier die SiP stacking assembly.

Table 1
Dimensional parameters of the SiP structure.

Number of tiers	Component	Length (mm)	Width (mm)	Height (μm)
1	Die	4.1	4.1	120
2	Die	3	3	120
3	Die	4.1	4.1	120
4	Die	3	3	120
1	Adhesive film	4.1	4.1	37.5
2	Adhesive film	3	3	30
3	Adhesive film	4.1	4.1	30
4	Adhesive film	3	3	37.5
–	Package substrate	7	7	600
–	Molding compound	7	7	800

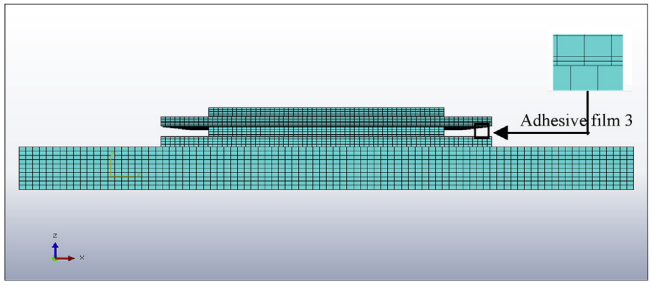

Fig. 2. Finite element meshed models.

Table 2
Mechanical parameters of the materials used in the FEA model [18–20].

Material	Young's modulus (GPa)	Shear modulus (GPa)	Poisson's ratio	Density (kg/m^3)
Die	165.5	/	0.25	2330
Package substrate	26 (X, Z) 11 (Y)	7.59 (XZ, YZ) 3.31 (XY)	0.39 (XZ, YZ) 0.11 (XY)	2000
Adhesive film	1.2	/	0.3	10,500
Molding compound	24.5	/	0.23	1900

Table 3
Thermal parameters of the materials used in the FEA model [18–21].

Material	Thermal conductivity (W/m K)	Specific heat (J/kg K)	Thermal expansion coefficient (10^{-6}/°C)
Die	153	703	2.3
Package substrate	0.51	920.9	15 (X, Y) 50 (Z)
Adhesive film	374	0.23	49
Molding compound	0.67	1050	10

substrate with a low elastic modulus enhances the drop performance. Regard et al. [13] reported a new acceleration stress test combining thermal stock and moisture storage and found that cracking is not independent of delamination since it occurs at the end of the delaminated zone. Although several reliability tests of the SiP structure have been conducted, relatively limited work has considered thinning the dies. The use of thinner dies minimizes the board standoff height by allowing the entire package to be thinner [14,15]. Normally, in a SiP structure with an overall height of 1.2 or even 1.0 mm, the thickness of each die in a 2-or-3-die stack is approximately 150–175 μm and is further reduced to approximately 75–100 μm in 4-to-7-die stacking applications [16]. Currently, the primary SiP structure format uses 3- or 4-die stacks; additional formats are in development or in low-volume production.

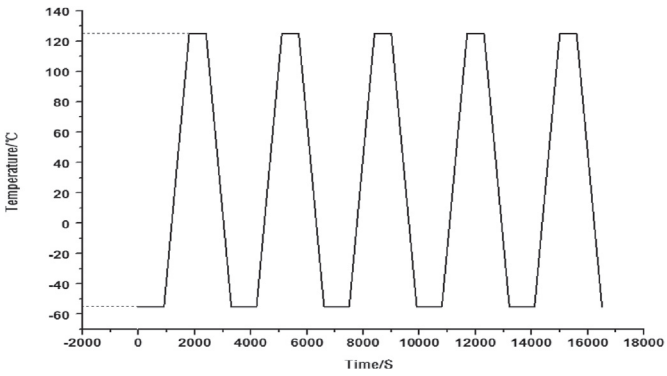

Fig. 3. Thermal cycling curve.

We designed a four-tier die-stacked SiP structure and used ANSYS software to simulate the thermal stress distribution within the die. Scanning electron microscopy (SEM) was used to observe the failure sites within the SiP structure, and the Taguchi optimization method was applied to obtain an optimal and robust design that enhances the thermal reliability of the four-tier die-stacked SiP structure.

2. Finite element simulation and thermal cycling test

2.1. Finite element modelling

The test vehicle used in this study is a four-tier ultra-thin-die SiP stacking assembly with the structural configuration shown in Fig. 1. The SiP structure containing four-tier dies, package substrate, adhesive film, and molding compound is made by Amkor and has a body size of 7 mm × 7 mm. The material dimension parameters of the components of the structure are presented in Table 1. The package substrate and molding compound are 7 mm × 7 mm in length and width, respectively. The thickness of the package substrate is 600 μm, and that of the molding compound is 800 μm. Two sets of die dimensions, 4.1 mm × 4.1 mm × 120 μm and 3 mm × 3 mm × 120 μm, are used. To simplify the calculations, non-essential factors are neglected in this work [17]. Fig. 2 shows the FEA model of the SiP structure, which contains 117,834 C3D8R elements and 129,816 DC3D8 elements. C3D8R is an 8-node linear brick element with reduced-integration points and leads to uncontrolled distortion of the mesh, and DC3D8 is an 8-node linear brick element without any control of the integration points. The analysis is conducted using ANSYS v.8.0.

To simplify the numerical simulation, all materials were assumed to be isotropic and homogeneous. Tables 2 and 3 list the mechanical and thermal parameters of the materials obtained from the suppliers along with references [18–21]. To evaluate the reliability of the four-tier ultra-thin-die SiP structure, thermal cycling loading ranging from −55 °C to 125 °C with a temperature change of 30 °C/min was applied to all nodes, as shown in Fig. 3. In the FEA model, the stress-free condition was assumed to be 25 °C. During thermal cycling, the stress and strain of most materials undergo cyclical changes. The stress and strain stabilize after several cycles [22,23]. Thus, in this study, a total of five cycles at 3000 s/cycle were modelled under the thermal cycling profile. At each specific time step, the temperature was assumed to be uniform across the

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