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A high stable 8T-SRAM with bit interleaving capability for minimization of soft error rate

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ABSTRACT

The impact of alpha particle and exposure to cosmic radiation has multifold the existing stability issue associated with modern sub-100 nm SRAM cell design. Noise insertion in the half selected cell of a SRAM array is another serious issue which degrades the stability of a cell as well as waste energy through the half selected cells. The proposed highly stable 8T-SRAM cell takes care of both the above mentioned issues effectively. The cell is capable to be arranged in a bit-interleaving fashion which can then use a conventional error correction code (ECC) to correct the single bit error caused by the exposer to cosmic radiation. Traditionally the read stability and write ability are conflicting to each other and any one of them can be enhanced with sacrificing the other. But the proposed cell enhances both the read stability and the write ability simultaneously. Two other cells namely the 8T differential (8T-DIFF) SRAM and 9T read disturbance free (9T-RDF) SRAM are compared with the proposed SRAM cell which consume 20.1% and 16.2% more energy respectively. The read speed of the proposed SRAM is significantly higher than the 9T-RDF SRAM and marginally higher than the 8T-DIFF SRAM. The write speed of the proposed SRAM is also better than the two compared SRAM.

1. Introduction

The performance of modern SOC is widely affected by the performance of on chip memory situated inside it. So designing high speed energy efficient robust SRAM have drawn huge research interest. Several techniques are proposed to achieve these requirements. Few of them are supply voltage scaling, gating of supply voltage during sleep mode [1], switching off un-accessed portion of the cache [2] and engaging multi-threshold CMOS devices etc. Among all these techniques supply voltage scaling is widely preferred because of its quadratic control over dynamic power and exponential control over leakage current [3].

But the miniaturization of modern device increases the impact of process variation which degrades the stability especially in sub-100 nm technology. Further stability is linearly controlled by the supply voltage. So the scaling of supply voltage to achieve power advantage in other hand makes the cell more unstable. SRAM operated at lower supply voltage having low critical charge Q_{CRIT} [4,5] are more prone to alpha particle radiation and cosmetic energy rays which can introduce soft error easily. Conventional error correction code (ECC) can be utilized to correct this soft error, provided the error is single bit in nature [6–8]. To ensure this the SRAM cell must be organized in bit interleaved manner.

Another challenge in robust SRAM design is to achieve high read stability without affecting the write ability. All the efforts applied on the conventional 6T-SRAM cell to improve both stability and write ability simultaneously are failed as these two requirements are conflicting in nature to each other. Improving one requirement unavoidably degrades the other one. Several works are presented in literature [9–13] which separates read mechanism from write so that the inter dependency between them can be avoided and both the requirements can be improved simultaneously. The insertion of extra logic to separate read and write mechanism does not allow them to insert further the logic required for bit interleaving. So though these cells maintain the cell read stability and write ability, but they cannot reduce the soft error rate.

In this work we propose a robust highly stable 8T-SRAM cell which is capable of bit interleaving. It also increases the read stability without degrading the write ability. High speed read and low energy consumption are other appreciable features of the proposed SRAM cell. Comparison with two other bit-interleaving capable SRAM cells namely the 8T-DIFF SRAM cell [14] and 9T-RDF SRAM cell [15] shows the performance

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improvement of the proposed SRAM cell in terms of energy consumption, stability and speed.

The proposed SRAM cell has the following advantages.

1. Capable of bit interleaving.
2. High read stability without degrading the write ability.
3. Higher speed of operation.
4. Low energy consumption.
5. No cells are in half selected mode and no energy loss for them.

The rest of the paper is organized as follows. Section 2 presents a background about the work. The working of proposed 8T-SRAM cell is described in Section 3. In Section 4 the performance indices are analyzed. Finally Section 5 presents the conclusion of the work.

2. Background

Conventionally the SRAM array uses shared word line architecture to access a particular row, due to its simple design. A simple and gate can be used to select a particular word out of several words present in a row. As the output of a single and gate drives a complete word hence all the bits of a word must be placed adjacently. Keeping all the bits of a word adjacent to each other though makes the design simpler it increases the risk of multi bit soft error, particularly in sub-100 nm process technology. It significantly degrades the yield of chip. An alternate arrangement which interleave the consecutive bits of a word is hence preferred to avoid multi bit soft error. As shown in Fig. 1(b) in bit-interleaving architecture, 1st bits of all the words present in a row are placed adjacently and then all the 2nd bits and so on instead of placing all bits of 1st word and then 2nd word. Hence any ionized radiation when focused on the SRAM, can disturb only a single bit of a particular word instead of several bits of a single word unlike the case of shared word line architecture. The conventional ECC can be used here to identify and correct the single bit error. Implementation of bit interleaving architecture has a special requirement to select the bits of a word independently.

Half selected cell disturbance is another prominent drawback of the shared word line architecture. The activation of the shared word line, dedicated for a particular row, undesirably activates all the cells present in that row. All the cells experiences an undesirable dummy read current flow from their corresponding bit lines. This dummy read current should be restricted to avoid disturbance in the stored data and energy loss.

Do Anh et al. have proposed an 8T-SRAM cell [14] (see Fig. 2a) which meets the requirement for bit interleaving and eliminates the half select cell issue. It uses one extra inverter to activate the access transistor of a particular cell independently. This additional inverter is powered by a column selected line and 'WL' (Word Line) signal is given as an input to this inverter. Though this cell meets the requirements for bit interleaving and eliminates the half selected cell issue still it suffers from noise insertion problem during read. To solve the read disturbance issue, it increases cell supply voltage of the read column dynamically during read operation. But when the cell supply voltage is increased, the '1' node of all the cells in that column will be charged to the new supply voltage level. Again when the cell supply voltage comes back to normal level, all the '1' nodes of that column will be discharged to the normal level. This charging and discharging of all the '1' nodes of a column adds a significantly large power component to the existing requirement of power for normal read operation.

Liang Wen et al. have proposed a 9T-SRAM cell [15] (see Fig. 2b) which uses the same inverter concept to select the individual cell independently. It uses an unsymmetrical inverter pair as basic storage element. Data is written to the cell from one side with deactivating the feedback loop of inverter pair. Data is read from the other side through another access transistor. As the feedback loop is deactivated during read operation, the noise inserted to the internal node does not put the data at the risk of flipping. But when the cell completes read operation and enters to hold mode, the feedback loop is activated and the noise already inserted during read operation may increase the risk of flipping of the data node. Hence the use of one extra transistor to read the data with feedback loop cut off does not solve the read disturbance issue but increases area overhead. In addition to this, in 9T-RDF SRAM as the read access transistor of all the cells in a row are controlled by a common 'RWL' (Read Word Line), the half selected cell disturbance still persists during read operation.

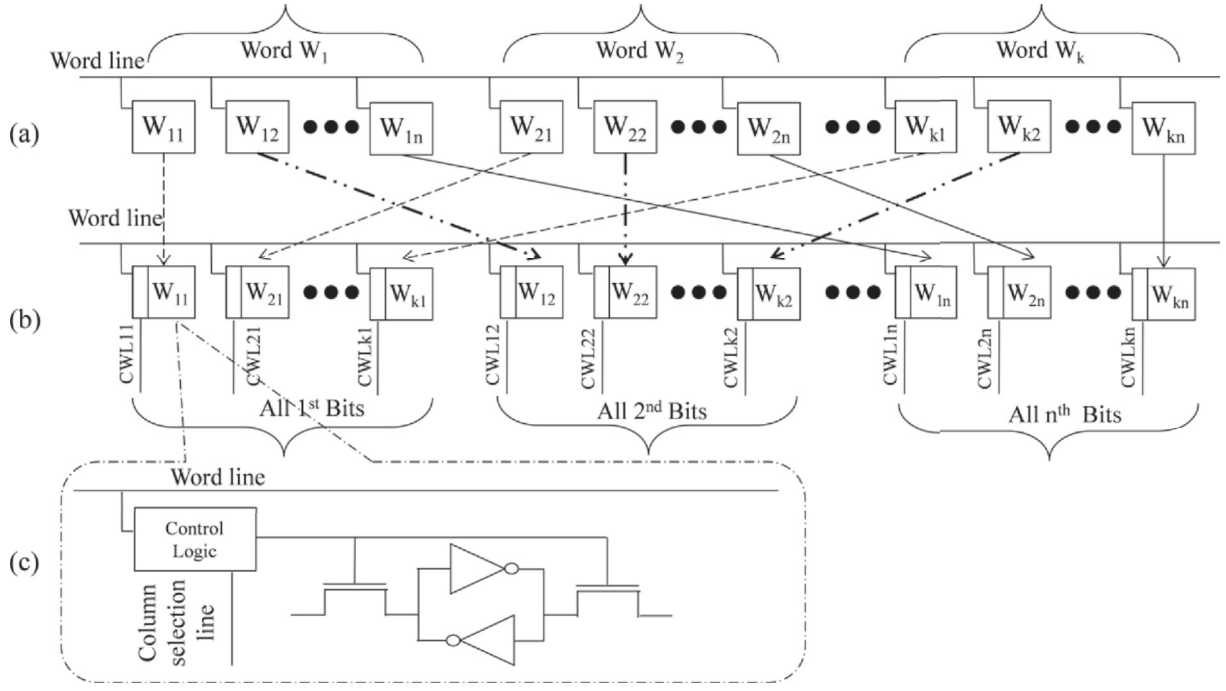

Fig. 1. (a) Shared word line architecture (b) Bit interleaving architecture (c) Requirement for bit interleaving.