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A reconfigurable dual-output buck-boost switched-capacitor converter using adaptive gain and discrete frequency scaling control

Libin George [a,*], Torsten Lehmann [a], Tara Julia Hamilton [b]

[a] School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW 2052, Australia
[b] The MARCS Institute, Western Sydney University, Penrith, NSW 2751, Australia

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ABSTRACT

This paper presents the design of a dual-output reconfigurable buck-boost switched capacitor converter architecture that can be adapted for applications requiring multiple, distributed on-chip loads. This system uses adaptive gain control and discrete frequency scaling to regulate power delivered. Core-interleaving, an enhanced load regulation scheme, and adaptive switch-sizing control have also been adopted to improve performance. The converter provides a fully-integrated, low-area and fully digital solution. Design and implementation using a standard bulk-CMOS 0.18 μm process provide simulation results showing that the converter has an output voltage range of 1.0–2.2 V, can deliver up to 7.5 mW of power to each load, and is up to 67% efficient, using an active area of only 0.06 mm^2.

1. Introduction

Advances in modern portable electronics have propelled the demand for smaller power supplies with versatile power management techniques and/or new system functionalities. Contemporary Systems-on-Chip (SoCs) include a wide range of integrated circuits with different power requirements. The integration of diverse technologies requiring different supply voltage levels and noise constraints on a single die has increased the complexity of power delivery on silicon. Therefore, effective power distribution techniques for integrated multiple-load systems are becoming significantly more important. On-chip point-of-load power supplies are placed close to the load circuitry to reduce the effective impedance between load circuits and power supplies [1]. Techniques such as power network optimisation and placement of decoupling capacitors are a few of those proposed for efficient power delivery systems [2]. These distributed power systems must often cater to a wide range of operating specifications whilst also providing high power conversion efficiency and minimizing losses, both static and dynamic. The advantages of reconfigurable electronics have encouraged an extension of the design paradigm to include integrated analog electronics such as power supplies. We focus on reconfigurable DC-DC converters that can operate over a wide range of input and output conditions towards the evolution of fully reconfigurable mixed-signal SoCs [3–5]. This work focuses on the development of a reconfigurable power supply IC architecture that takes advantage of novel control schemes to improve system performance and power delivery to multiple, distributed on-chip loads.

Switched-Capacitor (SC) power converters require less die area than other standard power supplies, thus being low cost solutions. Also, advancements in nanometer technologies have enabled switching at higher frequencies with less power loss, making it possible to further reduce the area overhead compared with other types of regulators [6]. They are therefore a good option for low power, on-chip devices with light load conditions as they can be switched at high frequencies without compromising on efficiency. Multiple-output SC converters can take advantage of these benefits to provide power to distributed loads at lower cost, complexity and power losses. However, because SC converters are usually configured to achieve a particular conversion ratio, any changes to input voltage will require re-design. Reconfigurable SC converters can be used to provide multiple conversion ratios and eliminate this problem. This paper discusses the design of a reconfigurable buck-boost SC power converter that uses adaptive gain (AG) control for coarse control and discrete frequency scaling (DFS) for fine control of the output voltages. This work firstly improves performance of the converter in Ref. [7]: Interleaving cores and enhanced sampling and DFS control algorithms are used to improve output ripple voltage and load regulation. These proposed schemes enable finer and more efficient control of the output voltages. Secondly, it presents a modular dual-output

* Corresponding author.
E-mail addresses: l.george@unswalumni.com (L. George), tlehmann@unsw.edu.au (T. Lehmann), t.hamilton@westernsydney.edu.au (T.J. Hamilton).

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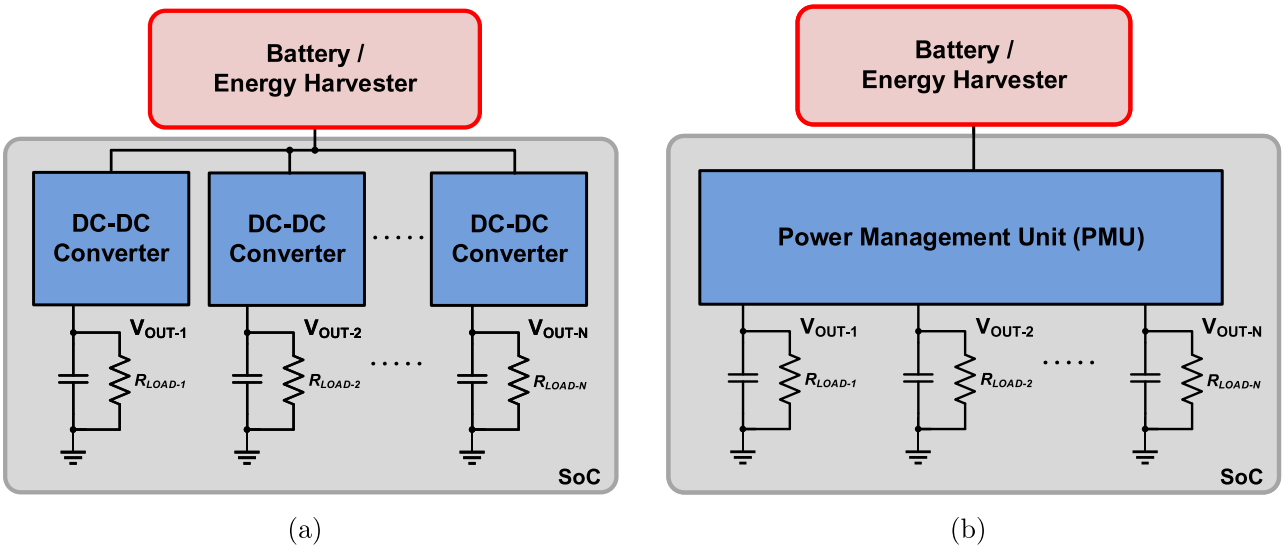

Fig. 1. (a) System block diagram of common SoC power supplies and (b) the proposed power management method.

system architecture that can be extended for more outputs, and can be adapted for multiple-load distributed SoCs such as multi-core systems operating with dynamic voltage and frequency scaling (DVFS) [8]. This architecture is better than [9] because it provides both buck and boost operation, uses less pump capacitors and switches, a better load regulation technique and contributes a low-area, fully-integrated solution that includes on-chip capacitors. As the control loops are predominantly digital, this system also has the advantage of being more compact and scalable and allows for the signals in the converter to be carried over larger distances to on-chip loads spread across a die. Section 2 discusses how multiple-output SC converters are beneficial in modern SoCs that often contain multiple loads of different types, distributed across a die.

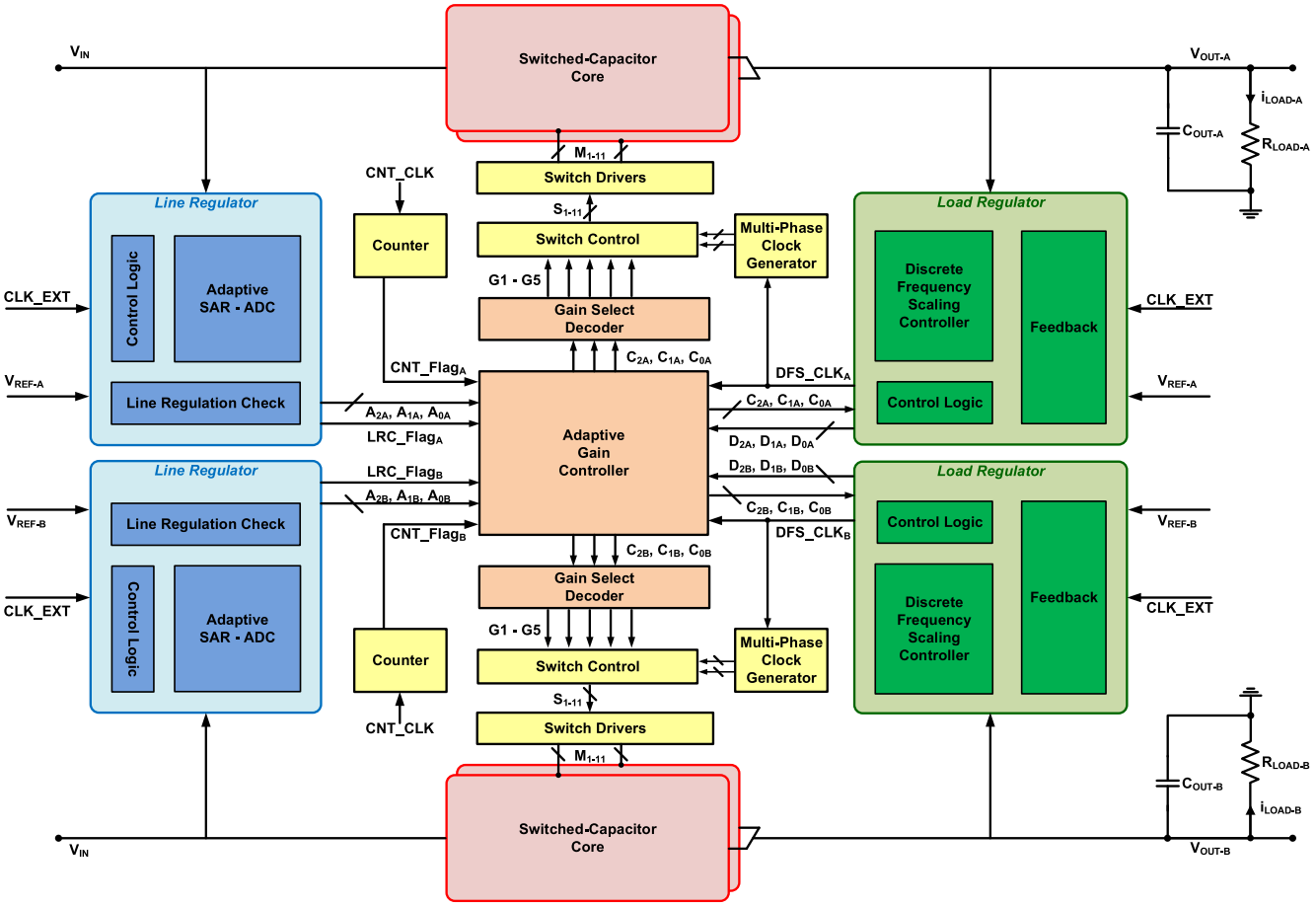

Fig. 2. System-level architecture of the proposed dual-output reconfigurable SC converter, modified from Ref. [15].