Microelectronics Journal 72 (2018) 14–23

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Design and implementation of a high-throughput configurable pre-processor for MIMO detections

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ARTICLE INFO

Keywords:
MIMO detection
Pre-processor
QR decomposition
MMSE
Systolic array
CORDIC

ABSTRACT

This paper presents the VLSI architecture and circuit implementation of a high-throughput multi-mode pre-processor for 4 × 4 MIMO detections. This design can be configured to perform pre-processing schemes including QR decomposition (QRD), Sorted QRD (SQRD), or MMSE-SQRD. Furthermore, in order to achieve high processing throughput, the proposed configurable pre-processor is architected based on the Givens rotation algorithm and a pipelined systolic array structure. Moreover, for reducing the hardware complexity and alleviating the overhead for configurability, several design innovations have been applied. Specifically, a novel norm-calculation scheme is utilized so that the overhead for the sorting operations is minimized. In addition, the utilized circuit elements are designed considering the hardware sharing paradigms. The proposed configurable pre-processor has been synthesized, placed, and routed using TSMC 90 nm technology. The post-layout estimations show that this design achieves a throughput up to 44M matrices per second for decomposing 4 × 4 channel matrix, outperforming prior works with equal functionality and architecture.

1. Introduction

Multiple-Input Multiple-Output (MIMO) technology has been widely recognized as a promising scheme for modern wireless communication systems owing to its high data rate and improved signal quality [1–3]. Furthermore, MIMO technology has been adapted into contemporary and next-generation wireless standards such as IEEE 802.11n/ac, 3GPP-LTE/LTE-Advanced, and 5G [4]. In general, the signal detector and channel decoder [5] are the two major processing components at the receiving end of a MIMO system, where the MIMO detector is responsible for recovering the originally transmitted symbols and the channel decoder retrieves source bits based on the results of the detector. Since the MIMO detection are involved with a number of complex-valued signal processing operations, it usually results in significant delays and high complexities. To be specific, the Maximum-Likelihood (ML) MIMO detector achieves an optimal solution in the sense of minimized Bit Error Rate (BER) at the cost of the enormous computational complexity [6]. Furthermore, it has been well known that the MIMO detection schemes based on tree-searching type algorithms can achieve close-to ML BER performance with greatly reduced complexity [7,8]. Therefore, it has been the design of choice since its debut. The tree-searching type MIMO detector is comprised of a two-stage operation, where a pre-processor constructs the tree structure and a tree-searching engine finds the shortest path in this tree [8]. In this scheme, the pre-processor typically performs a QR Decomposition (QRD) to convert the channel matrix into the product of a unitary matrix Q and an upper triangular matrix R [9,10]. Since the QRD is involved with a number of matrices and vectors operations, the pre-processor of the MIMO detector usually results in significant delays and occupies excessive hardware complexities in the MIMO receiver [11].

In addition, it has been reported in literature that the pre-processing scheme with advanced signal processing techniques improves the signal quality of detected results and enhances the efficiency of the tree-searching operation, especially when the wireless channel is ill-conditioned [12–14]. In particular, the pre-processor with sorted-QRD (SQRD) [12] approach contains the advantage that the detector identifies the close-to ML solution by searching a smaller subset of tree nodes compared to the conventional QRD-based pre-processor. Furthermore, applying the Minimum Mean-Square Error SQRD (MMSE-SQRD) further reduces the search space and thus enhances the efficiency of the MIMO detector [13,14]. Therefore, the pre-processor using SQRD or MMSE-SQR schemes have been widely utilized for improving the signal quality or enhancing the efficiency of the MIMO detector. Nevertheless, applying SQRD or MMSE-SQRD approaches also increase the delay and complexity of the pre-processor itself. As a result, the signal processing approaches that are employed for designing the pre-processor lead to a trade-off

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https://doi.org/10.1016/j.mejo.2017.10.004
Received 14 September 2016; Received in revised form 10 February 2017; Accepted 2 October 2017

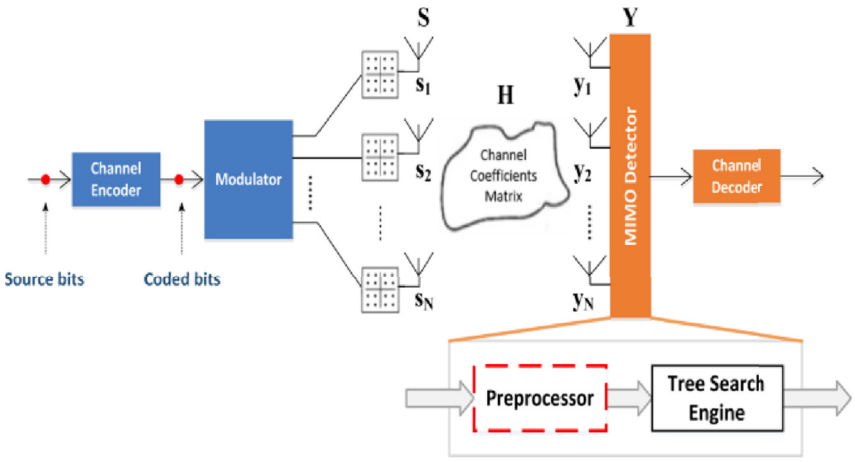

Fig. 1. The simplified system model of the MIMO communication system.

between the pre-processor and the MIMO detector. Specifically, advanced pre-processing algorithms improve the efficiency of the MIMO detector and the signal quality, at the cost of increased delay and complexity of the pre-processor. On the other hand, a simplified pre-processing scheme reduces the complexity of the pre-processor, while degrading the efficiency of the MIMO detector.

In order to strike a balance between the complexity and the signal quality of the pre-preprocessor and MIMO detector, it is essential to design and implement a multi-mode pre-processor structure that can operate different schemes in different channel conditions. To be specific, in the environment of good channel conditions, the pre-processor operates the less-complex QRD mode since it is sufficient for maintaining the quality of the signal, and thus leads to the minimal system overhead. On the other hand, when the channel is in the vicious condition, the pre-processor operates the SQRD or MMSE-SQRD modes, aiming to improve the quality of the detected signal. In order to achieve this goal, this paper presents the VLSI architecture and circuit implementation of a high-throughput configurable multi-mode pre-processor for 4 × 4 MIMO detections. This pre-processor is configurable to support three modes of pre-processing approaches including QRD, SQRD, and MMSE-SQRD according to the channel conditions. Furthermore, in order to enhance the processing throughput, the proposed scheme is designed in a pipelined systolic array architecture, where one channel matrix can be processed in every five cycles. In addition, for minimizing the overhead incurred by supporting configurability, several complexity-reduction techniques are applied for designing the architecture. In particular, each processing unit of the systolic array is specifically architected and optimized based on the designed operating functions. Furthermore, the hardware-sharing structures are employed so that hardware components are largely re-used when operating in different modes. Moreover, a novel norm-calculation scheme is utilized for minimizing the overhead of the norm-computation and sorting operations. The proposed configurable multi-mode pre-processor has been implemented using 90 nm technology and the post-layout estimations show that, when supporting the configurability, a throughput up to 44M matrix per second can be delivered.

2. Background and related works

2.1. MIMO system and pre-processor of MIMO detection

Fig. 1 shows a simplified mode for the considered MIMO wireless communication system assuming the dimension of N × N. In this model, the transmitter sends an N × 1 signal vector **S** and the receiver receives an N × 1 vector **Y** given by

$$\mathbf{Y} = \mathbf{HS} + \mathbf{n} \tag{1}$$

where **H** represents the N × N channel matrix and **n** is the N × 1 noise vector. It has been shown that the tree-searching based MIMO detector can achieve a close-to ML BER performance with reduced complexity. In such scheme, a pre-processor is employed to construct the tree structure. Typically, the pre-processor performs QR-Decomposition (QRD) to convert the channel matrix **H** into a product of a unitary matrix **Q** and an upper triangular matrix **R** as follows

$$\mathbf{H} = \mathbf{QR}. \tag{2}$$

Thus, equation (1) can be re-written as

$$\mathbf{z} = \mathbf{Rs} + \mathbf{w} \tag{3}$$

where **z** is equal to $\mathbf{Q}^{\mathbf{H}}\mathbf{Y}$ and **w** is equal to $\mathbf{Q}^{\mathbf{H}}\mathbf{n}$. Furthermore, it has been shown in Ref. [21] that utilizing the Sorted QRD (SQRD) algorithm in the pre-processor can improve the BER performance of the detected signals. The SQRD scheme needs to calculate the norm value of each column vector and process column vectors based on the ordered norm value. Thus, the symbol with highest SNR is detected first so that the error propagation is minimized and the BER performance is improved. In addition, employing Minimum Mean-Square Error SQRD (MMSE-SQRD) [26] in the pre-processor can further improve the quality of the detected signals. The principle of MMSE-SQRD is to consider the additive noise through the construction of an augmented channel matrix $\overline{\mathbf{H}}$ as follows

$$\overline{\mathbf{H}} = \begin{bmatrix} \mathbf{H} \\ \sigma_n \mathbf{I_N} \end{bmatrix} \tag{4}$$

where $\mathbf{I_N}$ represents the N × N identity matrix and σ_n is the Gaussian noise. The MMSE-SQRD scheme improves the channel condition and thus the tree-searching engine improves the BER performance with a further reduced search space.

For instance, assuming a 4 × 4 16-QAM MIMO system, the BER performances of applying QRD, SQRD, and MMSE-SQRD pre-processing algorithms are summarized in Fig. 2. The K-Best structure [7,8] with K = 4 is utilized as the MIMO detector scheme. It is shown in Fig. 2 that the MMSE-SQRD scheme outperforms the QRD and SQRD, while SQRD also results in a better BER than the QRD. Although increasing the parameter K improves the BER performance of QRD and SQRD, it also enlarges the search space of the tree-searching operation and thus increases the complexity. However, the computational