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A 1.2 V, 3.0 ppm/°C, 3.6 μA CMOS bandgap reference with novel 3-order curvature compensation

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ABSTRACT

This paper presents a bandgap reference with a high-order curvature compensation circuit which can improve the temperature coefficient (TC) in a wide temperature range. The proposed compensation circuit includes a second-order and a third-order curvature current generators as well as an I-V converter. These two curvature currents are achieved by utilizing the exponential behavior of sub-threshold MOSFET and used for compensating the high-order temperature dependence of BJT base-emitter voltage via I-V converter. The proposed BGR is implemented in a CMOS 0.18 μm process with the active area of 0.056 mm^2. Measurements on ten samples showed that at the minimum supply voltage 1.2 V, the TC varies from 1.7 to 6.9 ppm/°C over a temperature range of 170 °C (−45 °C–125 °C) with an average value of 3.0 ppm/°C and the total current consumption of 3.6 μA at room temperature. In the supply voltage range of 1.2–1.8 V, the line regulation (LR) is 0.025%/V.

1. Introduction

Bandgap voltage references are critical building blocks for CMOS integrated circuits and widely used in analog circuits, digital circuits and mix-signal integrated circuit. For example, the TC accuracy of the voltage reference has an important impact on the resolution and conversion speed in ADC and DAC circuits.

Because conventional bandgap references (BGRs) are implemented by the common-collector structure of the parasitic vertical bipolar junction transistor (BJT) [1,2], the minimum supply voltage should be higher than 1.25 V to ensure the normal work of the circuit. With requirements of low voltage and low power for portable electronics products, the methods proposed in Refs. [3–14] achieve a sub-1 V reference voltage by using resistive subdivision methods.

Since first-order temperature compensated in conventional BGR, the performance of temperature coefficient (TC) is limited by the nonlinear dependence of the base-emitter voltage (V_{BE}). In order to improve the TC, several curvature compensation techniques have been developed in Refs. [5–17] which obtain a good TC (1–10 ppm/°C) over a wide temperature range. In Refs. [5,6], High-order temperature compensation is achieved by generating non-linear current using transistors (BJTs) flowing through different current densities. The bias current in the compensation circuit is mirrored on the BGR core in Ref. [6], resulting in a large power consumption. Piecewise-nonlinear curvature compensation technique has been proposed in Ref. [7] and adopted in Refs. [8–10]. The method of this technique is generating compensation current in the different temperature ranges to be integrated at the output of a first-order BGR in order to compensate its nonlinear behavior. However in Ref. [9], the compensation current is large, so that the power consumption of the entire circuit is large. In Refs. [11,18,20], a temperature-dependent resistor ratio generated by a high-resistive poly resistor and a diffusion resistor is used to provide the high-order compensation. This compensation method has the advantages of simple architecture and low power consumption. However the temperature characteristics of the resistors are directly affected by the process. Some curvature-compensation technique are propose in Refs. [12–14], which generate second-order curvature currents using special circuit structures to achieve second-order temperature compensation. However, The BGR circuit in Ref. [12] consists of two BGR cores which increases the chip area and power consumption. And the circuits in Refs. [10,13,14,19] use MOS BGR which always suffer from degraded performance in accuracy due to the MOS transistor threshold voltage

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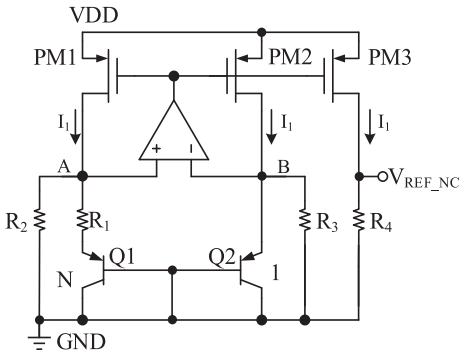

Fig. 1. Schematic of the basic low-voltage BGR.

(V_{TH}) changes a lot under process variations. Another curvature compensation method was proposed in Ref. [21], where its circuit structure is uncomplicated and works in the nanoampere current consumption range. However this method is poorly robust. Because the TC accuracy lies on a matching between V_{TH} and V_{BE} which is extremely hard to achieve.

Based on the high-order compensation circuit introduced in Ref. [15], this paper proposes a 3-order curvature compensation. The proposed technique generates second-order and third-order curvature currents to compensate the BGR high-order temperature dependence in wide temperature ranges. The experimental results indicated that the proposed technique can achieve a good TC over a wide temperature range with the average TC of 3.0 ppm/°C and the proposed circuit dissipate current of 3.6 μA at 1.2 V supply.

This paper is organized as follows. section 2 presents the low-voltage BGR and the basic concept of curvature compensation. The proposed BGR circuit is discussed in Section 3. Section 4 shows the simulation and measurement results. The conclusion is given in section 5.

2. The low-voltage BGR and the basic concept of curvature compensation

2.1. Low-voltage BGR

As shown in Fig. 1, the basic low-voltage BGR is conventional first-order compensated CMOS bandgap reference [5]. The operational amplifier forces the voltage at node A and B to be equal. The voltage across R_1 is equal to the difference value between V_{BE1} and V_{BE2}, called as ΔV_{BE}, which can be described as

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln N \tag{1}$$

where $V_T = k_B T/q$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge and N is the emitter area ratio of Q1 and Q2. In this paper, the closely packed common-centroid layout is adopted. Due to the logarithm relation, the large N does not provide significance change so that N = 8 is chosen based on the consideration of the chip area.

Because the *P1, P2* and *P3* have the same W/L ratios, the current I_1 in *P1*, *P2* and *P3* is same and is given by

$$I_1 = \frac{\Delta V_{BE}}{R_1} + \frac{V_{BE2}}{R_2} = \frac{V_T \ln N}{R_1} + \frac{V_{BE2}}{R_2} \tag{2}$$

Since the reference voltage output can be written as

$$V_{REF\_NC} = I_1 R_4 = \frac{R_4}{R_2}\left(\frac{R_2 k_B \ln N}{q R_1} T + V_{BE2}\right) \tag{3}$$

For a BJT, the base-emitter voltage V_{BE} can be expressed as

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{4}$$

where I_S is the saturation current of the bipolar transistor. Because V_{BE} is generated from a p-n junction diode with a negative TC, Eq. (4) can be approximated as [16].

$$V_{BE} = V_{G0} - \gamma T \tag{5}$$

where $V_{G0} \approx 1.2$ V is the bandgap voltage of silicon, γ is the temperature coefficient of V_{BE}. Its value is approximately −2 mV/°C at 300 K. In order to achieve first-order compensation, the value of $R_1 k_B \ln N/(qR_0)$ is equal to −2 mV/°C.

2.2. Curvature-compensation method

The PTAT voltage is used to cancel out temperature dependence of V_{BE} in basic BGR. As Eq. (5) is approximated by the first order, TC is typically zero at one temperature point and positive or negative at other

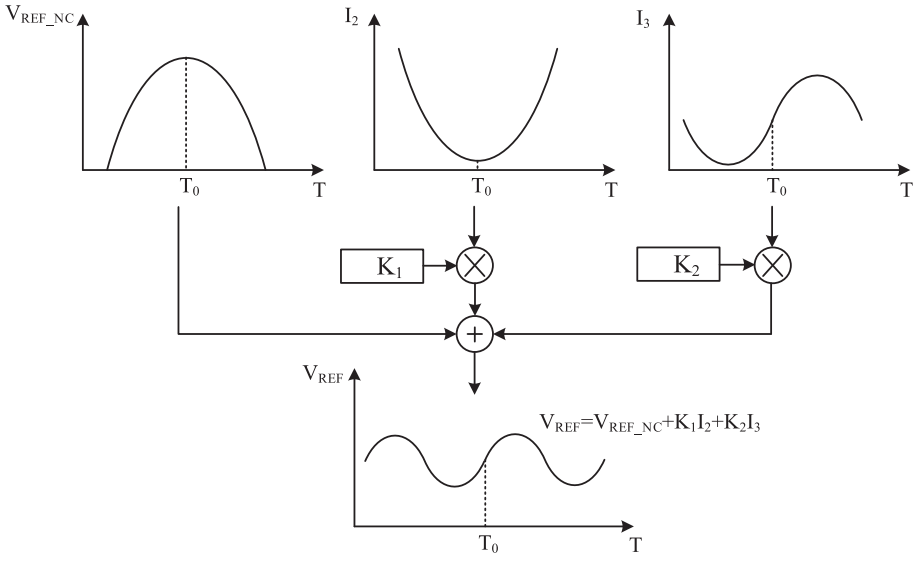

Fig. 2. Curvature compensation principle.