



Memristor-CNTFET based ternary logic gates

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ABSTRACT

Multilevel electronic systems offer the reduction of implementation' complexity, power consumption, and area. Ternary system is a very promising system where more information is represented in the same number of digits compared to the binary systems. In this paper, ternary logic gates and some of their ternary circuit applications are presented using memristors and CNTFET inverter. This integration between memristors and CNTFET offers low static power, small area and high performance. The proposed circuits do not require refreshment like the previously published circuits and are not initial state dependent because the memristors switch between the low resistance and high resistance states according to each input. In addition, we investigate the mathematical analysis of the proposed memristor ternary logic gates circuits. In the circuit simulations, a VTEAM model is used to verify the proposed circuits. Finally, a comparison between the proposed circuits with the previously published implementations is discussed showing better performance in terms of power, delay and area.

1. Introduction

The memristive devices and systems theory has been postulated for the first time in 1971 by L. Chua [1,2]. But, it did not gain the researchers' interest until HP announcement of finding this missing device in 2008 [3]. Later, different devices were introduced to match the applications demand such as frequency, nonlinearity, switching, and threshold current/voltage dependency [4–12]. These properties attracted the researchers' attention and promised the memristor to be used in different applications in both analog and digital domains. The analog behavior of the memristors can be utilized in multilevel discrete systems such as memristive ratioed logic (MRL) and threshold logic [13,14], fast switching memory [15,16], programmable logic array [17,18], digital binary computational components [19–24], reconfigurable computing [25], pattern recognition [26], image processing [27] and biological brain neuron network [6], [28]. The tiny size the switching behavior of the memristors promoted as an alternative device to the transistor-based memories because the transistors are reaching the physical limits [29, 30].

The conventional digital systems are built based on the binary numbers where only two levels are considered; zero and one. Recently, the concept of the multi-valued logic became a common research topic, especially with the existing devices that motivate the multi states [31]. In 1950s, Russians developed a computer system “SETUN” based on the

ternary numbers as the multi-valued logic [32]. The main advantage of ternary number is that it provides more information to be represented in the same number of digits compared with binary numbers which reduces the complexity of interconnection and the chip area [2]. Also, it can be used to implement high speed algorithms for arithmetic operations such as redundant numbers [33–37]. There are two representations for the ternary numbers; the unbalanced representation where only positive voltage levels are used as {0, 1, 2}, and the balanced representation where both positive and negative voltages are used as {−1, 0, 1} [34–37]. In 1980s, the first implementation of ternary logic gates is introduced based on CMOS using enhancement and depletion transistors [33]. Despite of using CMOS to implement ternary numbers which reduces the power dissipation, it has a highly sensitivity to transistor dimensions. Later, the researchers tried to implement convenient ternary numbers logic gates based on carbon nanotube field-effect transistors (CNTFETs) [38]. A single-wall carbon nanotube (SWCNT) can be emerged as a conductor or semiconductor depending on the angle of the atoms' arrangement along the tube. CNT devices are considered as an alternative to MOSFET devices [38]. The CNTFET's properties are totally controlled by the tube's diameter. Moreover, CNTFET enhances the power and the delay compared to CMOS transistors [39]. But, CNTFETs suffer from “charge pile-up” in the channel that affects the performance of on/off switching [39]. In this work, we utilize the memristors to build ternary components due to their ability for fully switching [13] and tiny

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area [40]. Fig. 1 shows the structure of both memristor and CNTFET transistor.

Recently, ternary numbers gates were implemented utilizing the multi-states ability of the memristors using the simplest HP model [41] which is not practical and does not represent the realistic devices' behaviors. Moreover, in Ref. [41], the design needs refreshment circuits for returning the memristors to their initial states. More realistic models should be used in the implementation which consider the practical behavior of the memristors such as VTEAM [42]. In this paper, both memristors and CNTFETs are used to build compact and reliable logic circuits. Ternary logic gates are introduced and analyzed. Then, these basic logic gates are used to build digital ternary blocks for arithmetic ternary operations [33] based on the different design methods such as ternary K-map and the threshold-adaption methods. The design using threshold-adaption method is introduced for the first time to build the logic circuits. Finally, a comparison between the proposed circuits and different design methods is introduced and discussed. Also, a comparison between the proposed circuits and CNTFET-based circuit is introduced in terms of power, energy, delay and estimated area.

This paper is organized as follows: Section 2 proposes the concept of the ternary memristive logic gates circuit. The circuit realization and the numerical simulation for the proposed circuits are introduced in Section 3. Section 4 discusses the realization of the ternary gates using the memristors and CNTFET. Section 5 presents building different blocks based on ternary Memristor-CNTFET gates. The conclusion is drawn in Section 6.

2. Proposed memristive logic gates circuits

One of the models that achieves the digital circuits' properties is the voltage threshold adaptive memristor (VTEAM) model [42]. It has the same properties of TEAM model which became widely used due to its simplicity, generality, accuracy, and low computational complexity [43]. Due to the desire of using the threshold voltage in some application, VTEAM has been created. Soon after, it became convenient in digital applications [42]. The governing equations of the VTEAM memristor can be simplified as follows:

$$\frac{dx(t)}{dt} = \begin{cases} k_{on} \left(\frac{v_m(t)}{v_{on}} - 1 \right)^{\alpha_{on}} & v_m \leq v_{on}, \\ 0 & v_{on} \leq v_m \leq v_{off}, \\ k_{off} \left(\frac{v_m(t)}{v_{off}} - 1 \right)^{\alpha_{off}} & v_m \geq v_{off}, \end{cases} \quad (1)$$

$$v_m(t) = R_m(x, V)i(t) = [R_{off}x(t) + R_{on}(1 - x(t))]i(t), \quad (2)$$

where x is normalized internal state variable, $v_m(t)$ is the voltage across the memristive device, k_{on} and k_{off} are constants, v_{on} and v_{off} are mem-

ristor threshold voltages, α_{on} and α_{off} are nonlinearity coefficients, $i(t)$ is the current passing through the memristive device, R_{on} and R_{off} are the minimum and maximum memristance respectively. By differentiating the memristance in (2) relative to time and substituting into (1), the rate of change in the memristance is

$$\frac{dR_m}{dt} = R_d \begin{cases} k_{on} \left(\frac{v_m(t)}{v_{on}} - 1 \right)^{\alpha_{on}} & v_m \leq v_{on}, \\ 0 & v_{on} \leq v_m \leq v_{off}, \\ k_{off} \left(\frac{v_m(t)}{v_{off}} - 1 \right)^{\alpha_{off}} & v_m \geq v_{off}, \end{cases} \quad (3)$$

where $R_d = (R_{off} - R_{on})$. A numerical solution for (3) can be obtained by applying Euler method. The memristance can be given by

$$R_m(j+1) = R_m(j) + \Delta t R_d \begin{cases} k_{on} \left(\frac{v_m(j)}{v_{on}} - 1 \right)^{\alpha_{on}} & v_m \leq v_{on}, \\ 0 & v_{on} \leq v_m \leq v_{off}, \\ k_{off} \left(\frac{v_m(j)}{v_{off}} - 1 \right)^{\alpha_{off}} & v_m \geq v_{off}, \end{cases} \quad (4)$$

where Δt is the time step. The memristive circuit that used to perform ternary gates consists of two series memristors as shown in Fig. 2. The voltage across each device is:

$$v_{d1} = R_{eq1}I_1 \text{ and } v_{d2} = R_{eq2}I_2, \quad (5)$$

where v_{d1} and v_{d2} represent the voltage drop across the two memristors. And I_1 and I_2 show the current passed through the whole circuit in Fig. 2, thus (5) is represented as following:

$$\frac{v_{d1}}{v_{d2}} = \frac{R_{m1}}{R_{m2}} = \frac{v_{in1} - v_0}{v_0 - v_{in2}}, \quad (6)$$

Then, the output voltage at instant j is given as

$$v_o(j) = \frac{R_{m1}(j)v_{in2}(j) + R_{m2}(j)v_{in1}(j)}{R_{m1}(j) + R_{m2}(j)}, \quad (7)$$

The time domain solution of the circuit can be obtained by solving Equations (7) and (4) numerically. Some devices such as [39] has low threshold voltages (v_{on} and v_{off}) where the devices switch after these thresholds. By using this property, the resistance of the device is either R_{on} or R_{off} which can facilitate the analysis. For $v_m < v_{on}$ and $v_m > v_{off}$, the memristance, R_m , is R_{on} and R_{off} , respectively. Therefore, the ternary-OR and Ternary-AND gates can be obtained as follows:

2.1. Ternary-OR gate

The definition of TOR function represented as (8) and Fig. 3 shows its circuit using memristor using the memristive MAX circuit which is

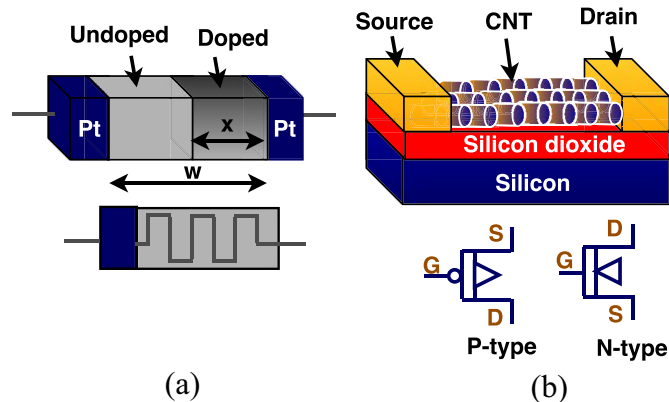


Fig. 1. Structure model of (a) memristor, and (b) CNTFET.

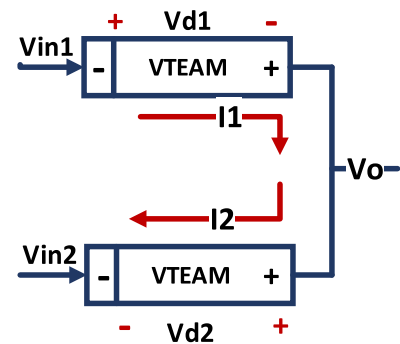


Fig. 2. Memristive gate circuit.

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