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Dual material gate nanowire field effect diode (DMG-NWFED): Operating principle and properties

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ABSTRACT

In this paper the impacts of warp-around gates on the electrical characteristics of a field effect diode (FED) have been presented in terms of I_{ON}/I_{OFF} ratio and gate delay by a numerical simulator. Simulation results show that quantum confinement effects result in nanowire regular FED (NWRFED) does not meet the drive current requirements predicted by the international technology roadmap for semiconductors (ITRS). By employing the gates with a different workfunction, we propose a "dual material gate nanowire FED (DMG- NWFED)" structure which supports the drive current requirements predicted by ITRS. Numerical simulations show that the subthreshold slope (*SS*) of the proposed structure is 53 mV/dec. In addition, the I_{ON}/I_{OFF} ratio in DMG-NWFED is approximately thirteen orders of magnitude bigger than I_{ON}/I_{OFF} ratio in NWRFED. The proposed structure provides a negative differential resistance (NDR) characteristic for 7.5 nm channel length and 3 nm nanowire diameter. This perhaps renders DMG-NWFED a prominent candidate for multilevel digital circuit applications due to its NDR characteristic.

1. Introduction

Complementary metal oxide semiconductor (CMOS) technology has been the leading technology for integrated circuit (IC) fabrication. However metal oxide semiconductor field effect transistor (MOSFET) devices are approaching their scaling limits due to the short channel effects (SCEs) [1–3]. Many approaches have been suggested to suppress the SCEs in MOSFET devices [4–9]. To decrease SCEs, new device structures are being explored to replace the conventional MOSFET devices [10–14]. Among them, field effect diode (FED) has been embraced by several researchers, partly because its fabrication procedure is similar to CMOS processing [15–19].

Fig. 1 shows the planar FED devices. We define the channel length as $L_{g1} + L_{g2} +$ the spacing between the two gates. The regular FED device is a pin diode in which the potential in the intrinsic region is controlled by two gates over the channel [13]. Unfortunately, the regular FED provides high OFF-state current for the channel lengths less than 75 nm and thus the device does not turn off [15–17]. To overcome this shortcoming the same group suggested a new structure which they called modified FED (M-FED), see Fig. 1(a) [14]. In this structure, they employed a p^+ and an n^+ reservoirs in the source and drain respectively to causes hole injection to the sub-gate, close to source, and electron injection to the sub-gate, close to drain respectively, in the off mode. In this manner the n^+pnp^+ structure will develop and the device will turn off. In Ref. [16] a simpler structure side contacted FED (S-FED), S-FED device shown in Fig. 1(b), was suggested. However considering band to band tunneling (BTBT) in Vadizadeh et al. [18,19], showed that neither the S-FED nor the M-FED's channel length can be scaled down below the 35 nm. BTBT strongly depends on the tunneling barrier width. The barrier width in lateral direction depends on the channel length for both S-FED and M-FED devices. For devices shown in Refs. [14] and [16], tunneling occurs at a distance greater than 25 nm from the surface. Upon scaling, electron direct tunneling from source to drain dominates in the OFF-state and leakage current increases. Furthermore, extra steps are inevitable to form reservoirs at source/drain regions for both the M-FED and S-FED devices. Also, due to the demand for very shallow source/drain regions, M-FED and S-FED fabrications may not be feasible.

Using an oxide layer in the channel is proposed to enhance the control of the gates on the channel carriers. We called this structure, shown in Fig. 1(c) silicon on raised insulator FED or in short SORI-FFD. In Ref. [18], we have shown that the SORI-FED device provides channel length scaling possible down to 20 nm. However, in SORI- FED device, the formation of oxide step in the channel makes the fabrication process difficult. By employing germanium in the channel, source and drain regions, as well as a silicon doped layer in the channel, the modified hetrostructure FED (MH-FED) has been suggested, Fig. 1(d) [19].

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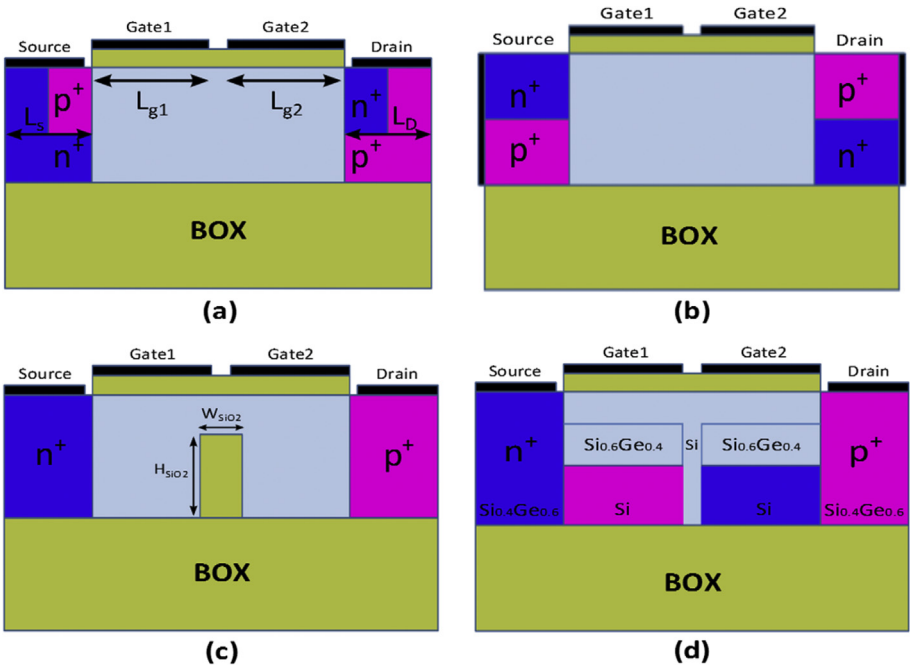

Fig. 1. (a) M-FED, (b) S-FED, (c) SORI-FED and (d) MH-FED. The structural parameters of the planar FEDs (i.e. M-FED, S-FED, SORI-FED, and MH-FED) in Refs. [14,16,18,19] are as follows: The space between two gates is 5 nm, the L_S=L_D = 85 nm, the gate oxide thickness is 2 nm and body thickness is 50 nm.

MH-FED structure decreases BTBT deep in the device channel. However, in MH-FED device, applied biases to Gate1 and 2 will not modulate the barrier height at the source/channel and drain/channel junctions for channel length below 25 nm [19]. Thus, the barrier heights decrease. This is reflected in a high OFF-state leakage current and hinders the device turn off.

In this paper, the "nanowire regular FED (NWREFD)" has been considered to reduce the SCEs in FED devices. Based on applied biases to the gates, source, and drain contacts, there are three ON-state modes and two OFF-state modes for planar FEDs [16]. In this study, we have investigated the operational principles of NWRFED as a possible candidate to replace the planar FEDs in the nanometer regime, assuming that the *C* mode is used in the ON-state and the *E* mode is used in the OFF-state [16]. Simulation results show that the ON-state current of NWRFED device, does not meet drive current requirements predicted by international technology roadmap for semiconductors (ITRS). The aim of this work is to modify the NWRFED structure to increase the ON-state current for the channel length below 20 nm. Numerical simulations have shown that, if gate workfunction engineering (e.g., by replacing the metal gates of NWRFED with the gates having different workfunction) is employed, the NWRFED is assembled to dual material gate nanowire FED (DMG-NWFED), the ON-state current increases. Surveys performed in this study presented that the proposed structure shows the negative differential resistance (NDR) characteristic for 7.5 nm channel length and 3 nm nanowire diameter. We will also compare electrical characteristics of DMG-NWFED against NWRFED using two metrics: I_{ON}/I_{OFF} ratio, and gate delay parameters.

This paper is organized as follows: the details of the proposed structure are explained in Section 2. Section 3 describes the simulation method based on non-equilibrium green's function (NEGF) approach. In Section 4, the results of simulation are discussed. Finally, in Section 5, a conclusion will be provided.

2. Device structure

The DMG-NWFED device is a pin diode in which the potential in the intrinsic region is controlled by two gates with different work functions over the channel (see Fig. 2(a)). The device structure consists of a silicon

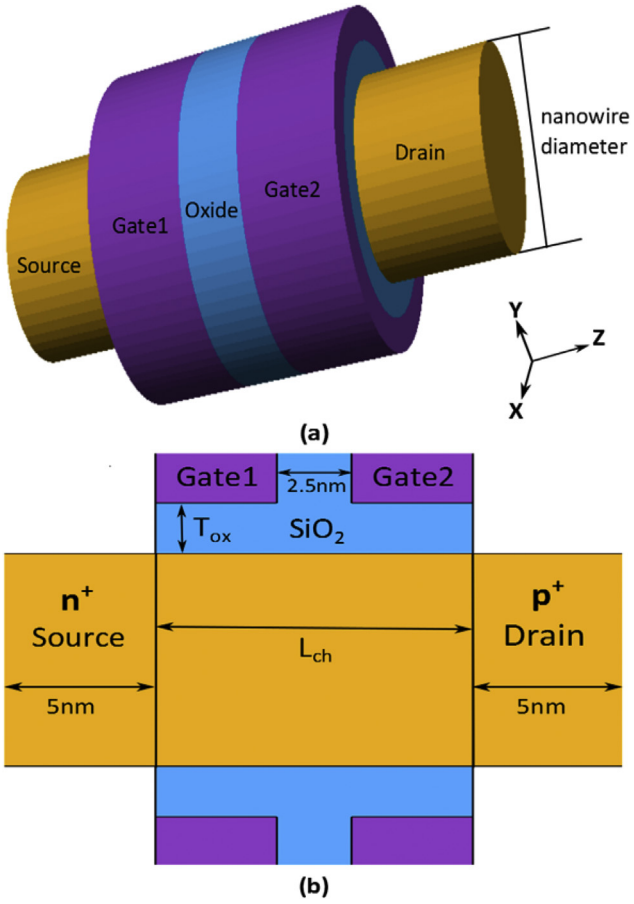

Fig. 2. The proposed structure investigated in this study. (a) Schematic view and (b) cross section view.