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A novel biasing technique for low phase noise voltage controlled oscillators

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ABSTRACT

This paper proposes a new biasing technique for LC-based voltage controlled oscillators to improve the phase noise performance while ensuring the current variations to be within an acceptable range. The proposed technique uses a feedback loop and a LDO to generate, sense, and regulate the output current. The oscillator has 33.3% tuning range around a center frequency of 2.4 GHz. The proposed design achieves −127.2 dBc/Hz phase noise at 1 MHz offset from 2.25 GHz while consuming 3.36 mA from a 3.3-V supply. The circuit was implemented in 65 nm UMC CMOS process. The results show that the circuit has *FoM* of −183.8 dBc/Hz and FoM_T of −194.5 dBc/Hz at 1 MHz offset, and the current variation across PVT is within +68 μA to −63 μA range.

1. Introduction

Voltage Controlled Oscillators (VCO) are widely used in many applications ranging from low-frequency function generators to high-frequency RF synthesizers. In this paper, a VCO is designed to be used in a frequency synthesizer to provide a stable local oscillator signal for RF transceivers. Major design challenges in VCO design are achieving low phase noise, low cost (area), and low power consumption. Among these, phase noise performance is the most critical design specification, which generally draws a limit for the minimum area and power consumption that can be achieved.

Although recent improvements in CMOS processes provide many benefits such as reduction of area, cost and power consumption for digital circuitry, analog and RF circuitry do not necessarily follow the same trend. VCOs are the best examples for the circuits that suffer from these enhancements. Firstly, the trend of lowering the supply voltage limits the VCO oscillation amplitude, which in turn has a negative impact on the phase noise performance. Secondly, the technology scaling increases the flicker noise generated by the devices and they exhibit worse thermal noise performance due to the higher noise factor (technology dependant factor). Furthermore, these devices tend to generate more harmonics, which results in low offset phase noise degradation due to the Groszkowski effect [1]. Finally, quality factor of the on-chip inductors are reduced in recent technologies, which again deteriorate the phase noise performance of all integrated LC oscillators.

Extensive research efforts have focused on the compromise between the best possible phase noise performance and the other design metrics mentioned above [2]. One study employs a high frequency VCO followed by a frequency divider to concurrently optimize the occupied area and the phase noise [3]. This solution is based on the fact that inductors can often achieve higher quality factor with smaller area at high frequencies. However, the reasoning is only valid if the added complexity of higher frequency VCO and high frequency divider designs do not overcome the savings in the occupied area and the consumed power. Moreover, the frequency divider may have a detrimental effect on the overall phase noise performance.

Phase noise analyses given in the studies [1,4,5] prove that the LC-VCO current source has a major contribution to overall phase noise due to its flicker and white noise. To mitigate this, a noise filtering technique was proposed in [6] by introducing an inductor and a large capacitor to filter the noise contribution of the current source. As a result of the different bias approaches presented in [7], the current source biasing approach along with the noise filtering technique provides a first-rate phase noise performance. Although the technique presented creates high impedance at the tail current source to reduce the up-converted flicker noise and filters the current source thermal noise around the second harmonic, the filter components increase the chip area significantly.

Another approach eliminates the tail current source altogether to improve the phase noise as proposed in [8]. Furthermore, it exploits the fact that the cross coupled transistors will self-bias when connected to the supply directly. Although this approach has many benefits regarding the phase noise performance, it suffers from uncontrolled current

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in the VCO. The current has to be chosen to meet the VCO requirements when it is minimum across PVT. Therefore, it causes the current to increase considerably in nominal conditions or corners where the current is maximized. In this work, the aforementioned technique is exploited along with a novel biasing technique to operate the VCO with negligible current variations across PVT. As a corollary, a robust low phase noise LC-based CMOS VCO is proposed.

2. Proposed architecture

The LC-based CMOS oscillators as illustrated in Fig. 1(a) offer many advantages over the conventional LC-based (NMOS-only and PMOS-only) oscillators. For the same current, it can achieve higher loop gain and offers better phase noise performance [4,5]. Leeson's equation given by (1) explains the phase noise in LC-based oscillators [4].

$$\mathcal{L}(\omega_m) = \frac{4KTRF}{V_1^2}\left(\frac{\omega_o}{2Q\omega_m}\right)^2, \tag{1}$$

where $\mathcal{L}(\omega_m)$ is the total phase noise at a frequency, ω_m, offset from the oscillation frequency ω_o, Q is the quality factor of the tank, and R is the resistive loss. V_1 is the oscillation amplitude and is proportional to the bias current within the current-limited regime as given by (2). On the other hand, the oscillation amplitude is constant and limited by the supply voltage in the voltage-limited regime. K is the Boltzmann's constant, T is the temperature in Kelvin, and F represents the noise figure of the oscillator as given by (3) [4].

$$V_1 = \frac{4}{\pi}RI, \tag{2}$$

$$F = 1 + \frac{4\gamma IR}{\pi V_1} + \frac{4\gamma g_{m,bias}R}{9}, \tag{3}$$

$$F = 1 + \gamma, \tag{4}$$

where γ is a technology dependent parameter, the bias current is represented by I, and $g_{m,bias}$ represents the transconductance of the current source transistor. Equation (3) takes into account the frequency translation of all the noise and the non-linearity effects. The first term represents the generated noise by the resonator. The noise generated by the differential pair, which is independent of the differential transistor sizes is given by the second term. The last term corresponds to the noise generated by the current source transistor.

When the oscillator operates at high current levels with moderate to high tank quality factors, the noise of the current source dominates the phase noise performance through (3). Since the current source is always kept in saturation region in conventional oscillators, the available headroom for the oscillation amplitude, V_1, is limited, which also leads to phase noise degradation as given by (1). Consequently, the current source has a major contribution to the overall VCO phase noise. If this contribution is removed from (3), the equation converges to its minimum value as given by (4). Although the oscillator can achieve the minimum noise figure as well as minimum overall phase noise in the absence of the current source as shown in Fig. 1(b), it suffers from undetermined bias current across PVT. In addition, the bias current can decrease too low and give rise to start-up failure. On the other hand, it can increase to a value that exceeds the limit of achieving the optimum phase noise or prohibit the use of the VCO in low power applications. The proposed design uses a LDO with a feedback loop in order to adjust the sum of V_{gs} drops across the PMOS and NMOS transistors to minimize the current variation across PVT. As a result, the current source in the design can be eliminated while regulating the bias current. Fig. 2 shows the block diagram of the proposed technique.

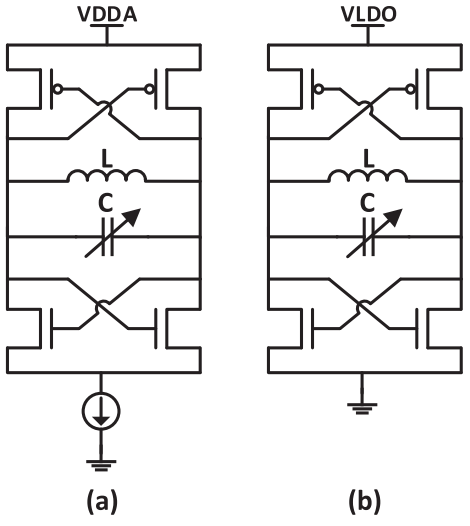

Fig. 1. VCO core schematic. (a) Conventional LC CMOS VCO schematic. (b) The proposed LC CMOS VCO schematic.

2.1. VCO core

The proposed VCO core schematic is shown in Fig. 1(b). From Leeson's equation (1), the most important step of VCO design is to choose the inductor that gives the highest quality factor (Q), regardless of the VCO topology used. Moreover, the maximum tank resistance R_p is desirable to maximize the oscillation amplitude V_1, minimize the power consumption, and minimize the core transistors sizing. It is also worth mentioning that the inductance value is proportional to inductor area, hence as L increases, the area increases as well. Accordingly, the chosen inductance value (L) is 4 nH with a quality factor (Q) of 12. In design, worst case scenario of R_p should be taken in consideration to insure the start-up of oscillation. Therefore, the cross-coupled MOS transistor dimensions are chosen such that the transconductance (g_{active}) provides the equivalent negative conductance value (g_{tank}) required to sustain oscillation as given by (5).

$$g_{active} \geq \alpha g_{tank}. \tag{5}$$

By using a fair assumption of $g_{active} = 4g_{tank} = \frac{4}{R_p}$ to insure the oscillation start-up, we conclude that $g_{mn} = g_{mp} = 3.4$ m℧. Now, the dimensions of the core devices can be easily calculated.

2.2. VCO capacitor DAC

In order to cover the desired frequency tuning range from 2 GHz to 2.8 GHz as well as to cover for PVT variations, a capacitor DAC is utilized in addition to a single varactor used for continuous tuning. This approach also helps keeping a moderate value of K_{vco}. A single switch is used for each capacitor bank in the DAC to switch both differential capacitors as depicted in Fig. 3(a) to minimize the resistive loading effect [9]. With differential swing at the switch terminals, only half of its on-resistance appears in series with each unit capacitor as shown in

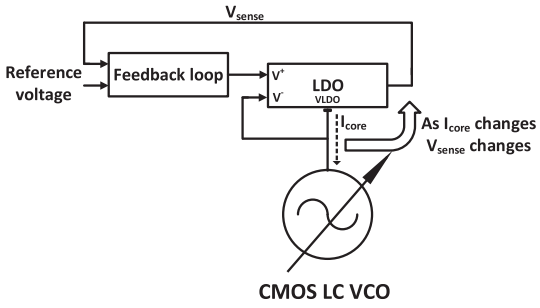

Fig. 2. The proposed VCO biasing technique.