Microelectronics Journal 71 (2018) 30–36

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 750-nW 1-MHz 9-tap analog finite impulse response filter for wireless senor network chip

Xin Xin, Jueping Cai *, Ruilian Xie, Peng Wang

State Key Laboratory of Wide Bandgap Semiconductor Technology Disciplines, Xidian University, Xi'an 710071, China

ARTICLE INFO

Keywords:
Low power
Analog FIR filter
Subthreshold
Discrete-time analog computing

ABSTRACT

This paper presents a low power Finite Impulse Response (FIR) filter based on discrete-time analog computing. The analog FIR filter is first presented to deal with analog signal. To improve linearity, two-double boost technique is introduced in the sample and hold cells which are used to achieve delay-time function. Meanwhile, the four-quadrant voltage-mode multiplier consists of PMOS substract cell and combiner cell, which is independent of device parameters. To realize the shift registers function, the rotating switch matrix circuit is adopted controlled by phase shift clocks. All MOS transistors implemented in this architecture are biased in subthreshold region with a supply voltage of 0.6 V to reduce the power consumption. Simulation results show that the analog FIR filter dissipates 750 nW at 1 MHz sample frequency and the effective number of bits of the proposed analog FIR filter is more than 7 bits. Compared to the conventional digital FIR filter, power consumption is reduced by 72.22% at 1 MHz in a 0.18μm CMOS process.

1. Introduction

Due to limitations on available power in the wireless sensor network chip, the power consumption of every block becomes an important issue that must be taken into account in order to maximize the battery life in the design [1,2]. In the conventional method shown in Fig. 1, the analog signal is transformed to the digital signal though analog-to-digital converter (ADC), and then it is filtered by digital transversal FIR filter. However, there are two main drawbacks in this conventional communication method. Firstly, the power consumption of the digital parallel FIR filter is high since it uses a lot of wallace-tree digital multipliers and registers. However, for low power implementation, digital FIR filter typically use simpler array multiplier. Voltage overscaling (VOS) is another technology to improved energy efficiency for the digital systems. The key issue of VOS technology is how to satisfy the functionality (e.g., signal to noise ratio (SNR)) when the transient logic errors exist. As pointed out in Ref. [3], there is a sharp degradation in the SNR performance for the digital FIR filter when the supply voltage is scaled, which limits the energy improvements. In Refs. [4] and [5], algorithmic-noise tolerance (ANT) and embedded ANT (E-ANT) have been proposed for large scale ultra-low-power digital integrated circuit design with a probabilistic model of timing error rate or the date path decomposition (DPD) technology, which balances between energy savings and performance degradation. These algorithms are based the fact that the statistical nature of application-level performance metrics, such as SNR, probability of detection, and bit error-rate (BER), implies that the circuits need not be 100% correct as long as the application requirements are met. The probabilistic model of timing error rate [4] and E-ANT [5] can achieve greatly reduce hardware overhead and power consumption with the acceptable SNR. Secondly, high tap FIR filter must be used when narrow transition-band characteristics are required, which leads to more consumption and area [6].

In previous works [7–11], analog FIR filter deals with echo cancellation, equalization or inter-symbol interference entirely in the analog domain to match the channel. The delay-line FIR architecture suffers from two significant shortcomings. First, each sample-and-hold (S/H) amplifier samples during the hold phase of the preceding S/H in the chain, thus requiring two S/H cells for each filter tap. Second, S/H noise, offset, and error accumulate when the signal propagates along the delay chain. The magnitude of this error will increase as the number of taps increases [7–9]. The serial FIR architecture [10,11], based on an inverter with active-inductor load or all-pass stages as the delay cell of the tap delay line, suffers for two reasons: (1) the delay accuracy will change with process, temperature and supply change, which affect the frequency response of the FIR filter [12], and (2) the delay error will increase with filter taps increasing. In previous time-interleaving FIR architecture, an

* Corresponding author.
E-mail address: jpcai@mail.xidian.edu.cn (J. Cai).

https://doi.org/10.1016/j.mejo.2017.11.010
Received 7 July 2017; Received in revised form 27 September 2017; Accepted 20 November 2017

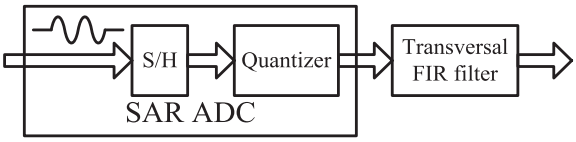

Fig. 1. The architecture of the conventional analog front-end circuit.

additional S/H stage is used to accommodate settling time requirements and reduce power [9]. The filter-x LMS algorithm is used to allow the equalizer to adapt and correct for the parasitic pole in the summation-node in high speed situation [13]. But this effect is not severe in the low-speed and low-power application. What's more, analog multiplier is achieved by multiplying digital-to-analog converters (MDAC) or Gilbert multiplier, resulting in the high supply and the high power consumption.

To address these issues, the design concept is proposed in this paper, which the function of digital circuits can be realized using analog circuits. Power consumption can be reduced since all analog blocks are biased in the subthreshold region and then the supply voltage of analog FIR filter is set to 0.6 V. Based on the design concept, this paper presents a design of the discrete-time analog FIR filter, shown in Fig. 2. A set of time interleaved parallel S/H cells are used to delay and store analog data signal. To improve linearity, two-double boost technique is introduced in S/H cell. The compact subthreshold multiplier is used to reduce power consumption significantly with PMOS substract cell and combiner cell. Meanwhile, the whole mismatch of the proposed multiplier can be designed and analyzed by considering the higher order terms and variations due to the process parameters. The rotating switch matrix circuit is adopted controlled to realize the shift registers function in FIR filter by phase shift clocks.

The contribution of this paper is as follow: Proposed FIR filter has a faster speed than [14], because the discrete time sampled signals are inputted to the multiplier directly while filter tap coefficients are fed to the multiplier by rotary switch matrix. Meanwhile, this method can suppress an accumulative switching error in analog samples due to rotating switch matrix. Compared with [14], the proposed analog FIR filter uses rotary switch matrix instead of the multiplexer, which greatly reduces the complexity of multiplexer, thus it reduces the power consumption and area. The proposed analog FIR filter is more suitable to the advanced process technology than digital counterpart, because of the low voltage and low power S/H cells and multipliers.

This paper is organized as follows. Section 2 describes the design concept and architecture of the proposed analog FIR filter. Section 3 provides the design and implementation considerations; Section 4, simulation results are shown and compared with low-power parallel digital competitors followed by conclusion in Section 5.

2. The proposed analog FIR filter architecture

Fig. 3 shows the proposed analog FIR filter's architecture and the operation timing based on discrete-time analog computing. The fundamental building blocks are S/H cells, analog multipliers, an adder and rotating switch matrixes. A fully differential architecture is used to suppress the substrate and supply noise and has good common-mode noise rejection. The x(t), C_k, x(n-k) and y(n) are the differential continuous-time analog signal, the differential filter coefficients, the delayed discrete-time sample signal and output sample signal, respectively. M-tap FIR filter performs the following convolution

$$y(n) = \sum_{k=0}^{M} C_k x(n-k) \tag{1}$$

The time delay function is implemented by using the time interleaved parallel S/H cells with different sampling phases. Repetitive multiplication is performed by the analog multipliers and rotating switch matrixes which are clocked sequentially by a series of the same even spaced clock signals, CLK0–CLKN-1(the same control as these S/H circuits). Compared to the digital adders, addition is operated by simply tying signals from the analog multipliers to a common node in the current-domain when one of the S/H is in tracking mode, which will reduce the power. Output current of analog multipliers can be converted to be filter output voltage by current-voltage stage or the diode-connected PMOS.

To relax the settling time of the S/H, N–M S/H circuits are used as redundant stages which increase power consumption. N–M equals one to balance between FIR filter speed and the power in our design. To achieve the same function as the M tap transversal filter, C_0–C_{M-1} and N–M zeros representing the tap coefficients multiply with the input samples. When the redundancy stage is in "sampling" state, the output of the corresponding S/H circuit will change timely, which will have an impact on the performance of the proposed filter. Furthermore, we control filter tap coefficients configuration though rotating switch matrix to make the input of corresponding multiplier of the redundancy stage equal to zero shown in the sequence diagram (Fig. 3), which avoids this impact.

The leakage power consumption may be a problem because of low power supply voltage in the design. When all the MOS are biased in the subthreshold region, the leakage power consumption will occupy the main part of power consumption. Then it has been discussed in the literature [15] that the leakage power consumption is smaller than dynamic power consumption of the MOS biased in the saturation region. The proposed approach cannot be pipelined, but it will not have an impact on the operation speed. The input signal is transmitted among the shift registers one by one in the conventional digital FIR filter design, but the input signal can be sampled at the same time by time-interleaved parallel S/H cells with the proposed method, which improves the operation speed in the low-voltage application.

This architecture offers four important advantages over the digital FIR implementations. Firstly, by applying low voltage four quadrant analog multipliers, it maintains low power consumption in the analog domain. Secondly, due to time-interleaving, it operates at a higher speed in the same supply voltage and technology. Thirdly, the proposed approach has a potential advantage in elimination of ADC, thus when ADC power is considered as part of overhead of the digital approach, proposed method can reduce the complexity and power consumption of the system further. Fourthly, to achieve the same or available SNR, the digital counterpart has to introduce the ANT, E-ANT or error resiliency, which is consist of detect and correct timing errors. However, the energy overhead of error correction eventually exceeds the energy savings from voltage scaling as the timing error rate rises [16,17]. More importantly, even if the VOS technology and the related algorithm are introduced, it is very difficult to achieve the same low supply voltage as the proposed architecture with the same SNR consideration.

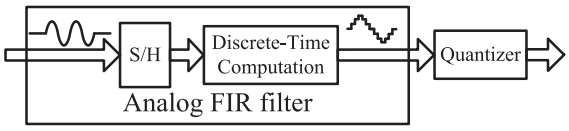

Fig. 2. The architecture of the proposed analog front-end circuit.

3. Analog FIR filter components

In this section, the fundamental building blocks of the proposed analog FIR filter such as S/H cell, the subthreshold multiplier, and rotating switch array are described. Because these blocks are crucial with regard to speed, power consumption, and accuracy of the entire analog FIR filter, much of the design concern was focused on designing and optimizing their performance.