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Stability analysis and compensation technique for low-voltage regulated cascode transimpedance amplifier

Behnam Abdollahi, Baset Mesgari, Saeed Saeedi *, Abdolreza Nabavi

Faculty of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran

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ABSTRACT

Stability of low voltage regulated cascode (RGC) transimpedance amplifier (TIA) with level shifter path is analyzed and criterions for a well-behaved time response are derived. It is shown that there is a trade-off between the amplifier bandwidth and stability in this topology. Improving bandwidth by increasing transconductance of transistors leads to ringing in the step response of the amplifier and finally its instability. To add a degree of freedom to design of the low-voltage RGC circuit for high-speed optical receivers, a compensation technique is proposed in this paper and employed in a TIA circuit, designed in a 0.18 μm CMOS technology. Post layout simulation results show a gain of 52 dBΩ and bandwidth of 3 GHz in presence of a 2 pF photo-detector (PD) capacitance and with power consumption of 4.3 mW. The results show that the proposed technique enhances bandwidth of the low-voltage RGC circuit by about 40%, while preserving its stability and well-behaved time response.

1. Introduction

Transimpedance amplifier (TIA) is a critical block in optical receivers, converting photo-detector (PD) current to an amplified voltage [1–5]. Large capacitance of PD usually creates a dominant pole at the TIA input and limits the amplifier bandwidth [6]. Therefore, input resistance of the TIA circuit should be sufficiently low to reduce the effect of the PD capacitance on the amplifier bandwidth. This issue is particularly important in wide-band TIAs designed in CMOS technology due to the performance limitations of transistors in this technology, such as relatively low transconductance and large parasitic capacitances [7].

To minimize input resistance of TIA in CMOS technology, regulated cascode (RGC) amplifier topology, which uses a gm-boosting technique in a common-gate stage for decreasing its input impedance, can be employed [1,8,9]. This topology is a popular TIA configuration due to its wide bandwidth and low power consumption. However, transistors in the basic RGC amplifier topology consume substantial voltage headroom and limit the amplifier performance at low supply voltages [6]. As design of TIA circuits at low supply voltages is critical for low-power and wideband applications, other low-voltage TIA topologies have been proposed and implemented in CMOS and BiCMOS technologies [3,10,11]. The common-gate (CG) topology with active feedback in Ref. [10] and the resistive shunt-feedback in Ref. [3] are low-voltage configurations, which decrease the input resistance of the CMOS TIA and reduce the effect of the PD capacitance on the amplifier bandwidth. However, employed PMOS transistors in these topologies increase the parasitic capacitance at the input and degrade the amplifier bandwidth. Regulated cascode (RGC) TIA with level-shifter path in Ref. [6] is a low-voltage configuration, alleviating the headroom issue in the basic RGC amplifier topology. This configuration has a higher gain compared to the active feedback circuit in Ref. [10] and lower input resistance compared to the resistive shunt feedback circuit in Ref. [3]. In this paper, stability of the low-voltage RGC configuration in Ref. [6] is analyzed and it is shown that the level-shifter path in this circuit leads to potential instability and imposes a severe constraint on achievable bandwidth in low-power and wideband designs. To benefit from high performance of the RGC topology and low-voltage operation of the level-shifter path, a compensation technique is proposed in this paper. It is illustrated that the proposed technique adds a degree of freedom for design of a stable low-voltage RGC TIA circuit, and enhances the amplifier bandwidth compared to the conventional RGC topology with level-shifter path. The bandwidth enhancement in the proposed topology is achieved without employing any inductor, which is usually used to improve bandwidth of TIA circuits [12].

* Corresponding author.P.O.Box: 14115-111, Iran.
E-mail address: saeed.saeedi@modares.ac.ir (S. Saeedi).

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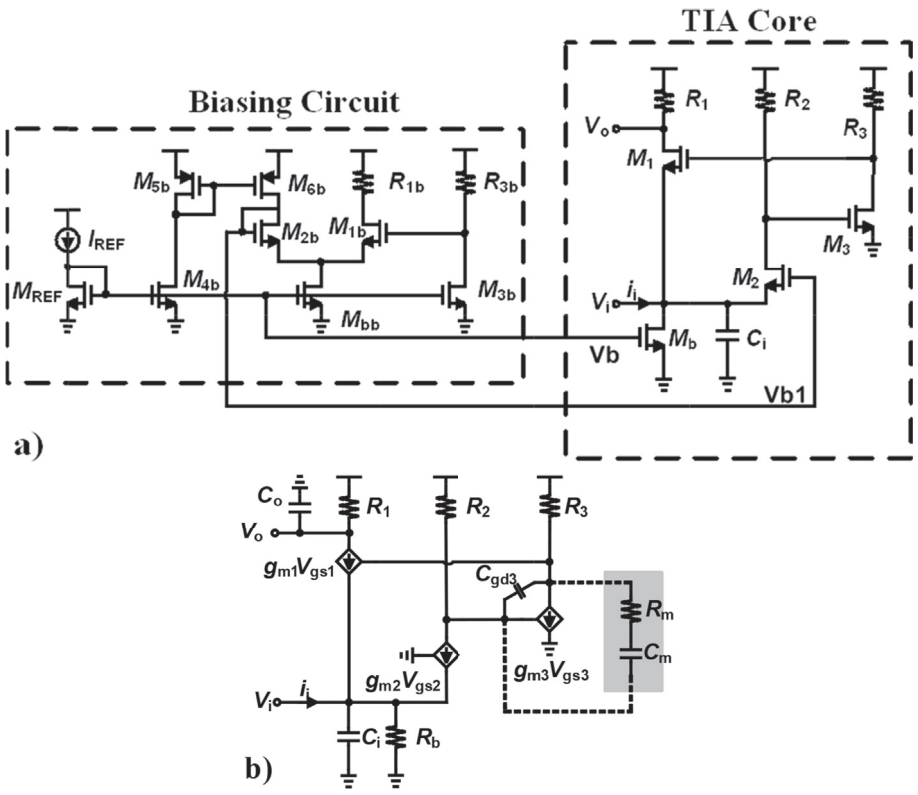

Fig. 1. a) Low-voltage RGC topology, b) Small signal equivalent circuit including the proposed compensation technique.

The paper is organized as follows. Stability analysis of the low voltage RGC circuit and criterions for its well-behaved time response are explained in section 2. The proposed compensation technique is presented in section 3. Performance improvement of the TIA circuit, employing this technique, is also analytically described in this section. Noise performance of the proposed circuit has been described section 4. To exemplify the proposed technique, a low voltage RGC circuit is designed in a 0.18 μm CMOS technology. Circuit design in this technology and post-layout simulation results are presented in section 5, followed by conclusions in section 6.

2. Stability analysis of the RGC circuit with level-shifter path

Fig. 1 a shows the conventional low-voltage RGC TIA circuit core [6]. It is a CG topology with a local feedback stage, which consists of the transistors M_2 and M_3 with their load resistors R_2 and R_3. The transistor M_2 shifts the gate voltage of M_3 to a higher level to reduce the required voltage headroom compared to the basic RGC topology. The transistor M_b is a current source for biasing the input CG stage.

For small signal analysis, the equivalent circuit in Fig. 1 b is employed. In this circuit, g_{m1}, g_{m2} and g_{m3} are transconductance of the transistors M_1, M_2 and M_3, respectively. The input and output capacitance, C_i and C_o in Fig. 1 b, as well as the parasitic gate-drain capacitance of the transistor M_3, C_{gd3}, determine the frequency response of the circuit. It will be shown that C_{gd3} generates a pair of complex conjugate poles and plays a key role in the stability of this topology.

Considering definitions and approximations in (1), input resistance and low frequency transimpedance of this circuit is expressed in (2) and (3), respectively.

$$\begin{cases} G_1 := (g_{m1}+g_{m2})R_b \\ r_1 := g_{m1}g_{m2}R_2R_3R_b \\ g_{m1} \gg g_{m2} \end{cases}, \begin{cases} G_2 := G_1 + g_{m3}r_1 \approx g_{m3}r_1 \\ r_2 := R_2 + R_3 + g_{m3}R_2R_3 \approx g_{m3}R_2R_3 \end{cases} \tag{1}$$

$$R_{in} = \frac{R_b}{G_2} \approx \frac{1}{g_{m1}(1+g_{m2}g_{m3}R_2R_3)} \tag{2}$$

$$Z_T = \frac{R_1(g_{m1}R_b + g_{m3}r_1)}{G_2} \approx R_1 \tag{3}$$

Definition of the four parameters in (1) and the related approximations are used to simplify other equations in the following sections and derive evident bandwidth expressions and stability criterions for the conventional and the proposed circuits. The approximations in (1) are reasonable in a wideband design with low power consumption. In particular, increasing the value of g_{m1} compared to g_{m2} in a power constrained design, as assumed in (1), results in a low input resistance with small increment of parasitic capacitances at the input. Therefore, it increases bandwidth of the TIA in Fig. 1.

Frequency response of the circuit, i.e. the transimpedance V_O/i_i versus frequency, is approximately derived from the following Laplace transform, H(s), by substituting the Laplace variable, s, with j2πf.

$$\frac{V_O}{i_i}(f) \approx H(s)\Big|_{s=j2\pi f} = \frac{Z_T\left(1+\frac{s}{\omega_{z0}}\right)}{\left(1+\frac{s}{\omega_{po}}\right)\left(1+\frac{2\zeta}{\omega_n}s+\frac{s^2}{\omega_n^2}\right)}\Bigg|_{s=j2\pi f} \tag{4}$$

The zero, real pole, natural frequency and damping factor of the response are expressed as

$$\omega_{z0} \approx \frac{g_{m2}g_{m3}}{C_{gd3}(g_{m3}-g_{m2})} \tag{5}$$

$$\omega_{po} = \frac{1}{R_1C_o} \tag{6}$$

$$\omega_n = \sqrt{\frac{G_2}{C_iC_{gd3}R_br_2}} \approx \sqrt{\frac{g_{m1}g_{m2}}{C_{gd3}C_i}} \tag{7}$$