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A frequency multiplier using three ambipolar graphene transistors

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ABSTRACT

In this paper, a frequency doubler circuit is designed using three ambipolar graphene transistors. Transistors are connected in series, across the voltage source (V_{DD}) and the ground (V_{SS}). Gates of transistors are shorted; a small AC signal is applied to the gate with a DC bias voltage. The output voltage signal is measured across the source and drain of the middle transistor. As the DC bias point is operated at the minimum-current voltage (V_{G_MIN}) of the middle transistor, single swing in the input causes double swing at the output. Furthermore, gates of three transistors can be shared as a common gate without using any connecting wire. Prior to the AC analysis, a DC sweep is performed to visualize the voltage change in each node. The required property of the ambipolar material for the implementation of the proposed circuit is also investigated.

1. Introduction

Frequency multiplication has always been used in various communication and processing applications, for example, fiber optics, point-to-point radios, measurement equipment, biomedical applications and radars [1–4]. There are several approaches of doubling the frequency. However, most of them can't maintain the exact wave-shape over a large frequency range without causing significant delay. As an example, class-C amplifier frequency doublers use inductors and capacitors and these components need frequency tuning. Voltage controlled oscillators (VCO) based frequency multipliers need several microseconds to provide a stable and accurate output. Diode-based full-wave rectifiers can double the frequency for a long range of input frequencies with the penalty of shape deformation [5]. Thus the ambipolar graphene FET is expected as the future candidate of the doublers can work at a higher frequency without the distortion of the wave-shape [6].

Several groups have designed ambipolar graphene FET based frequency multipliers, those can work at a larger frequency range, without significant delay and also requires no frequency tuning. However, most of their output curve is not purely sinusoidal and they used resistors, inductors or capacitors and those elements require a larger area to fabricate and need proper tuning [7–12]. The frequency doubling is also possible over a large frequency region with the graphene-based circuits using resistance load [7] but using a resistance corresponds to a larger area.

In order to solve these issues, we are proposing a circuit that can double the frequency, without distorting the wave-shape, consisted of only transistors and can be used over a large frequency range without tuning.

At first, we are showing the proposed circuit and DC simulation result. The mechanism is described with the help of DC simulation result in Section 3 followed by frequency analysis in Section 4. The reason for selecting graphene as the ambipolar material, instead of other ambipolar materials is discussed later in Section 5.

2. Proposed circuit and DC simulation

The proposed frequency doubler circuit consists of three ambipolar graphene transistors, connected in series with a common gate. Fig. 1a presents the I_{DS}-V_{GS} characteristics with different V_{DS} for a single ambipolar graphene transistor. Fig. 1b shows the proposed frequency doubler circuit diagram and Fig. 1c presents the current through transistors, node voltages (A, B in 1b) and the output voltage for the DC sweep.

During the DC simulation, the supply voltage V_{DD} is kept 1 V and the ground voltage V_{SS} is kept 0 V. The gate voltage is swept from 0 to 1 V for an easy visualization of current and voltages at different nodes. We used the model, derived by MIT [6] to simulate our circuit. HSPICE-netlist is used for implementing the circuit. Verilog-A file of the model is downloaded from the nanoHUB.

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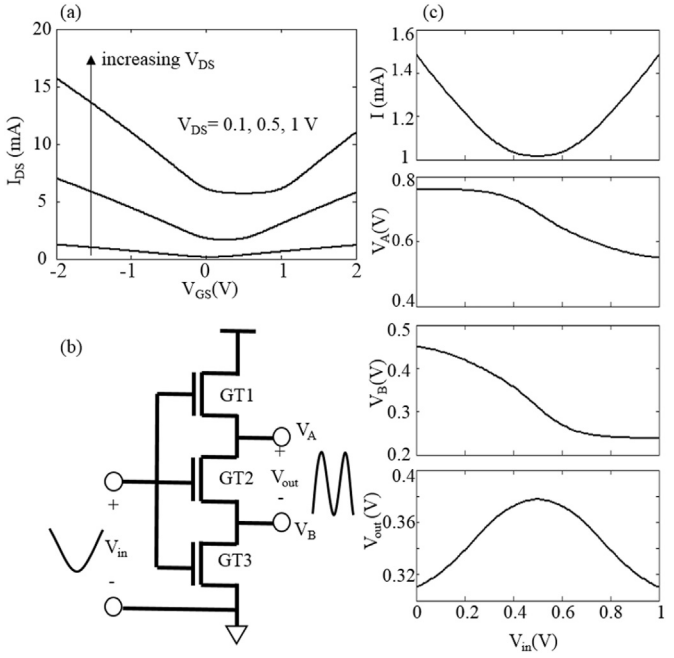

Fig. 1. The device, circuit and the effect of DC sweep on the output nodes (a) I_D-V_G curves for a single ambipolar transistor graphene. (b) Circuit diagram of the proposed frequency doubler, FETs (GTs) contains default values of the model [6]; i.e. W = 20 μm and L = 650 nm. (c) Drive current and voltages at A, B nodes and output voltage.

3. Working mechanism of the proposed circuit

The channel of ambipolar transistors carry mostly holes for a low gate voltage and carry mostly electrons for a high gate voltage. It is difficult to explain the relation between the current and the source, drain and gate voltages from the model equations [6]. Thus we are explaining situations with the help of the transfer characteristics, shown in Fig. 1a.

For a fixed V_D and V_S combination, current minima occurs at a medium gate voltage (i.e. $V_{G\_MIN} = (V_D + V_S)/2$). The current of the ambipolar transistor can be increased by increasing drain to source voltage (V_{DS}) or by increasing the difference between V_G and V_{G_MIN}. As a result, for a constant drain current, movement of V_G towards the minima (V_{G_MIN}) increases V_{DS} and vice versa.

As three transistors are connected in series, they contain the same amount of current. When the gate voltage V_{in} is close to 0 V, the value of V_G-$V_{G\_MIN}|_{GT3}$ is the lowest and the drain to source voltage of the GT3 ($V_{DS}|_{GT3}$) becomes highest among three transistors. As a result, both of V_A and V_B are high (Compared to V_{in}>0 situations). At $V_{in} = V_{DD}/2$ and for symmetric transistors, GT2 operates at its V_{G_MIN}. Thus the voltage across GT2 is the highest (i.e $V_{DS}|_{GT2}$>$V_{DS}|_{GT1}$, $V_{DS}|_{GT3}$). As $V_{out} = V_{DS}|_{GT2}$, the output voltage is the highest at $V_{in} = V_{DD}/2$. Similarly, V_A and V_B are low for high input voltage ($V_{in} \approx V_{DD}$).

According to the previous paragraph, the output voltage ($V_{out} = V_{DS}|_{GT2}$) is low for a low input voltage ($V_{in} \approx 0$), high for medium input voltage ($V_{in} \approx V_{DD}/2$) and again becomes low for high input voltage ($V_{in} \approx V_{DD}$). So a rise in the input voltage from 0 to V_{DD} will cause a rise and fall in the output voltage. Also, a fall in the input voltage from V_{DD} to 0 will cause a rise and fall in the output voltage. So, one rise and fall in input causes two rise and two fall in the output. Thus the frequency is doubled through the circuit.

4. AC simulation at different frequencies

According to the DC simulation, the output voltage goes to peak at the DC input of 0.5 V and the curve is also symmetric along the left and right side of this point. Thus, a constant bias of 0.5 V and an AC signal of 0.3 V amplitude is applied to receive a purely sinusoidal output. We also changed V_{DD} and found that, the DC bias point is $V_{DD}/2$ for identical transistors.

We simulated the circuit with different frequencies and the circuit with the default parameters of the model works up to 1 GHz frequency. Fig. 2a input signal (V_{in}), node voltages (V_A, V_B) and the output signal (V_{out}) for 100 MHz input frequency (f_{in}). Fig. 2b presents output signals (V_{out}) for input frequencies (f_{in}) of 1 GHz, 10 GHz and 100 GHz. According to Fig. 2b, the sinusoidal output starts distorting from 1 GHz with a slight difference between two adjacent peaks. At 10 GHz frequency that difference becomes more distinguishable, as the signal becomes distorted and the output fundamental frequency becomes equal to the input frequency. That happens due to the capacitance of the devices. A shorter channel length makes the channel resistance smaller, without increasing the capacitances. In fact, the channel to gate capacitances are decreased and other capacitances remain the same. That results in a decrease in the RC-delay. Thus, a shorter channel can support a higher frequency. We simulated the circuit with 10-times shorter channel length (65 nm) compared to the default values of the model and received improved high-frequency performance, shown as the last two subplots of Fig. 2b. Although the doubler is working at 100 GHz frequency with the smaller channel length, the signal is distorted at 1 THz frequency. However, the model contains the information of the separate source and drain for each transistor. When we are sharing the source and the drain of the middle transistor with others, the capacitances will be reduced.

5. Selection of the ambipolar material

Selection of ambipolar material is crucial for obtaining a sinusoidal output for a sinusoidal input signal. Thus, steep sub-threshold ambipolar devices are not suitable for the frequency doubler design. To prove that, we applied the Carbon Nanotube Field-Effect Transistor (CNTFET) model derived by ASU [13], where CNTFET have a steep sub-threshold. The current-voltage characteristics of a CNTFET is shown in Fig. 3a. The drain current changes logarithmically for the change in V_{GS} for a fixed V_{DS}. The drain voltage also changes logarithmically with the change of the V_{DS} and for a fixed V_{GS}. According to that model, CNTFETs are asymmetric, performance is not identical when the source and drains are flipped. Thus V_{DS} doesn't change symmetrically for the increase and the decrease of the

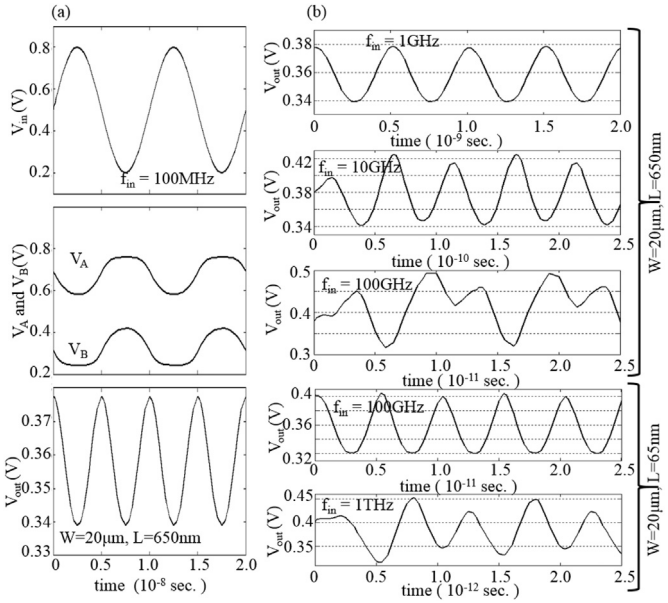

Fig. 2. AC simulation of the proposed frequency doubler. (a) Input signals, node (A, B) voltages, and output signal. (b) The output signal for the input signal of different frequencies and W/L.