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A 10-bit 1 MS/s segmented Dual-Sampling SAR ADC with reduced switching energy

Behnam Samadpoor Rikan [a], Hamed Abbasizadeh [a], Young-Jun Park [a], Hye-Yeong Kang [a], SangYun Kim [a], YoungGun Pu [a], Minjae Lee [b], Keum Cheol Hwang [a], Youngoo Yang [a], Kang-Yoon Lee [a,*]

[a] College of Information and Communication Engineering, Sungkyunkwan University, 2066, Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do 440-746, South Korea
[b] School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju 61005, South Korea

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ABSTRACT

This paper implements a 10-bit segmented Dual-Sampling SAR ADC for a WPT system. To solve the mid-code problem of the Dual-Sampling structure and improve the linearity, a segmented structure is adopted in capacitive DAC. A new switching scheme is proposed for MSBs decisions to skip some of the unnecessary switching steps. This ADC is applied to digitize analog inputs of the different sub-blocks of the WPT system. Applying these techniques reduces the unit capacitor size, as well as the power consumption while improving the linearity of the system. The overall system achieves 9.8 ENOB at 1 MS/s conversion speed and consumes 19.6 μA from 3 V supply voltage. DNL and INL for this structure are measured to be −0.63–0.56 and −0.85–0.79 LSB respectively. The active area of the ADC in 0.18 μm CMOS process is 760 × 430 μm^2.

1. Introduction

Wireless Power Transfer (WPT) technology has been studied and developed over the last few years because WPT systems offer high reliability, safety, and convenience. WPT is considered as a common interest in applications as diverse as biomedical implants, mobile phones, electric vehicles (EVs), LED TVs, and lighting. Recently, commercial products of mobile phone battery chargers have been successfully launched in the industry [1–3].

Analog to Digital Converters (ADCs) are extensively used in wireless sensor networks and healthcare electronic devices with medium resolution (8–12 bits) running at hundreds of kS/s to a few MS/s. It is essential in these applications to use an energy-efficient ADC to prolong battery life. A successive-approximation register (SAR) architecture, mostly composed of digital circuits, can achieve low power under low supply voltages [4–8]. Dual-Sampling is a structure that is used in industrial chips as a single-ended ADC structure. But similar to other binary switching structures, this structure usually has a problem in mid-code, which degrades the performance of the ADC [9,10].

This paper introduces an ADC with 8 inputs for different channels of the WPT structure. One of these inputs is applied for measurement purposes. The other inputs are applied to digitize the rectifier and DC-DC converter output voltages and currents. Foreign Object Detection (FOD) signal, internal and external thermal detection signals are other inputs. It applies 5 and 3 V supply voltages because the designed WPT system has two operating modes: the first one is AC supply input of the system, and the second one is battery mode. We provide a segmented Dual-Sampling structure with optimized switching sequence to solve the linearity problem of binary switching. Here, after MSB decision, thermometer codes are used to decide the next two bits. In addition, the switching sequence that we apply skips some of the unwanted switching steps.

This paper is structured as follows: Section 2 proposes the top architecture of this work, while Section 3 explains the proposed Core ADC structure. Section 4 presents the measurement results, and Section 5 concludes the paper.

2. Top architecture

Fig. 1 presents the simplified structure of the Power Receiver Unit (PRU) in a WPT system. As it is shown, the applied ADC has 8 inputs. One of these inputs (Test-IN) is used for test and measurement of the ADC. The other inputs are applied to digitize the Active Rectifier output voltage (V_{RECT}), Active Rectifier output current (I_{RECT}), DC-DC Converter output

* Corresponding author.
E-mail address: klee@skku.edu (K.-Y. Lee).

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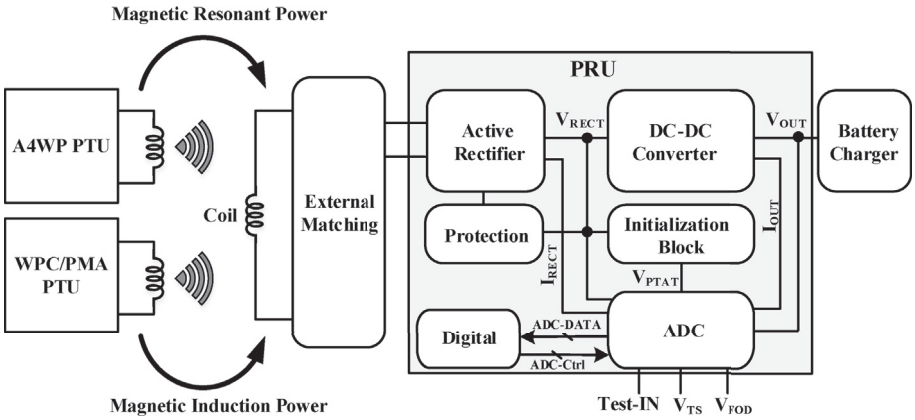

Fig. 1. Simplified structure of the PRU in the WPT system.

voltage (V_{OUT}), DC-DC Converter output current (I_{OUT}). FOD signal (V_{FOD}) is also digitized by ADC. This signal is applied to detect the foreign object between transmitter and receiver path. The internal thermal detection signal (V_{PTAT}), and the external thermal detection signal (V_{TS}) is also sensed and digitized through ADC. Besides, the ADC is applied in PTU part as well, with similar operation concept. ADC communicates with the digital part of the chip. The overall clock frequency of the system is 40 MHz and the maximum required conversion rate for the ADC in the designed WPT system is 1 MS/s.

Fig. 2 shows a top block diagram of the proposed SAR ADC. The ADC has 8 input terminals that are selected by the control signal (ADC_MUX<2:0>) from the digital block of the WPT system. The input range of the ADC block is 0.2–2 V. The Core ADC has a segmented Dual-Sampling structure. The input is sampled in both capacitive DAC and Sample-Cap. The Sample-Cap is divided into 4 parts. Three MSB capacitor values in capacitive DAC are 128C and decide the thermometer codes. In addition, an optimized switching technique skips some of the unnecessary switching steps, as will be described in the next section. A dynamic comparator is applied to the ADC. The comparator's clock is controlled by SAR logic and is only activated at each bit decision level. SAR logic also controls the capacitive DAC and Sample-Cap switching in each cycle. The reference generator provides the top reference voltage (2 V) and the bottom reference voltage (0.2 V). Trimming is applied to the reference generator to control the reference voltages in measurement levels.

Fig. 3 presents a timing diagram of the ADC. The clock frequency of the overall WPT system is 40 MHz. According to the required conversion speed of the ADC, the clock frequency divider (CLK Freq. Div. sub-block in Fig. 2) provides the proper clock frequency for the ADC (CLK-div). The system applies an active high reset signal (RST). ADC communicates with the chip's digital block by Start of Conversion (SOC) and End of Conversion (EOC) signals. B8 and B7 bits are decided using thermometer switching in capacitive DAC and/or Sample-Cap. This will be considered in Section 3.

The ADC resolution is 10 bits, and the clock frequency divider (CLK Freq. Div.) can determine the conversion rate. The input frequency to the SAR logic can be selected to be 5, 10, 20, or 40 MHz, so the conversion rate can be selected for 0.125, 0.25, 0.5, and 1 MS/s cases. The supply voltages are 5 and 3 V as mentioned before. In the charging mode when AC power is connected to the rectifier, the supply voltage will be 5 V in the overall system; but when battery mode is applied, the system, as well as ADC supply voltage, will be 3 V. The SAR Logic and digital parts of the chip apply 1.8 V supply voltage.

3. Core ADC structure and switching scheme

This structure applies a segmented Dual-Sampling SAR ADC. In Dual-Sampling structure, a single-ended input signal is sampled in both capacitive DAC and Sample-Cap. The first comparison is done without any switching energy. Switching sequence for a 3-bit Dual-Sampling structure is summarized in Fig. 4. After sampling at cycle 0, and holding at cycle 1, the MSB is decided. According to the MSB decision, the bottom plate of Sample-Cap will connect to V_{REF} or ground. For better performance of the ADC in terms of resolution and linearity, C_S size in Sample-Cap should be comparable and even same as the sum of all capacitors sizes in capacitive DAC. Therefore, for higher resolutions, this capacitor size is large. Hence, switching this capacitor consumes lots of

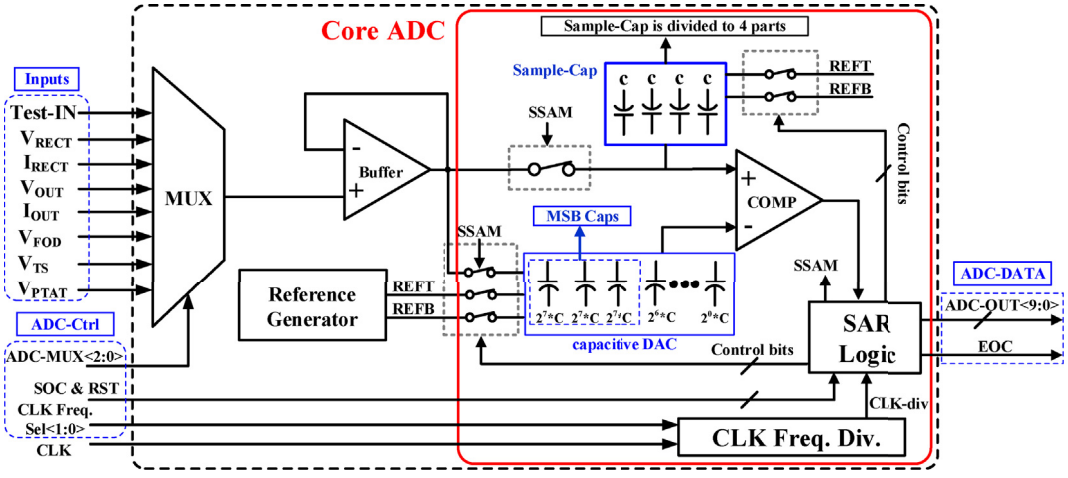

Fig. 2. SAR ADC top block diagram.