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High energy efficient analog compressed sensing encoder for wireless ECG system

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ABSTRACT

This paper proposed a high energy efficient analog compressed sensing encoder for wireless ECG system, where the input analog signal is multiplied by the random matrix and the products are integrated on the Multiplying Digital-to-Analog Converter/Integrators (MDAC/Is). Only one ADC is applied in this paper to sample 64 channels of MDAC/Is, compared with 64 channels of ADC in other design. Finally, the digitized measurement vector is obtained. The encoder was designed and simulated in a 0.13 µm CMOS process. Current leakages of the switches in MDAC/Is are cautiously considered. Several leakage suppression structures are employed. The leakage current in every switch is reduced to several fA. The average power consumption of the whole encoder is 23.5 µW. Signal-to-noise ratios (SNRs) of the reconstructed signal are 48.3 dB and 28.1 dB for Compressed Ratio (CR) = 2 and 4 respectively.

1. Introduction

Lots of noninvasive disease diagnosis methods have been presented in recent years [1,2], as patients' quality of care gains more and more attention. The body area network (BAN) promises quality of life improvements by making healthcare more accessible and removing the tethers associated with traditional medical telemetry systems [3]. Wireless body area sensors have been increasingly employed in medical monitoring, where high energy efficiency, small size and wireless telemetry are essential [4]. Our previous works [5–7] have investigated various researches on the small size of sensor node, compact practicability and multiple power control methods in wireless ECG system. This paper presents an analog compressed sensing system to reduce the power further.

Most power in a bio-signal sensor is dissipated when the RF power amplifier transmits data to the personal base station. Thus, it is desirable to decrease the amount of data transmitted and reduce the duty cycle of the transmitter [8]. This energy efficient paradigm is enabled using compressed sensing or compressive sampling (CS) in analog or digital domain wherein a compressible signal is acquired using only a few incoherent measurements [9]. CS theory states that signals sparse in some transform domain can be sampled at a lower rate than the Nyquist rate and can still be recovered without introducing distortions [10]. Prior research has shown that CS can be used successfully to exploit the sparsity of electrocardiogram (ECG) bio-signals [4,8,11]. Fig. 1(a) and (b) shows the block diagrams for digital and analog CS respectively. The drawback of digital CS is that compression algorithms are often sophisticated and require significant computational power and memory [12]. On the other hand, analog CS usually has 32 or 64 channels to obtain the output measurement vector [4,8], which also increases the chip cost and power consumption.

This paper proposes a novel analog CS system, which only applies one sub-Nyquist ADC to sample 64 channels of CS encoder (Fig. 1). The ADC only works during the sampling cycle and is turned off at most of the time. The leakage currents of the switched capacitors in MDAC/Is are carefully considered and suppressed. The system is designed and simulated in 130 nm CMOS technology. The simulation result shows a high efficiency and high accuracy to recover the original signal.

2. Compressed sensing

Compression with CS can be simply defined by the matrix equation:

$$[Y] = [\Phi][X], \tag{1}$$

wherein an uncompressed input vector $[X]$ of size N multiplied by a measurement matrix $[\Phi]$ of size $M \times N$ produces a measurement vector $[Y]$ of size $M < N$ [8,13]. Compressed Ratio (CR) can be calculated as:

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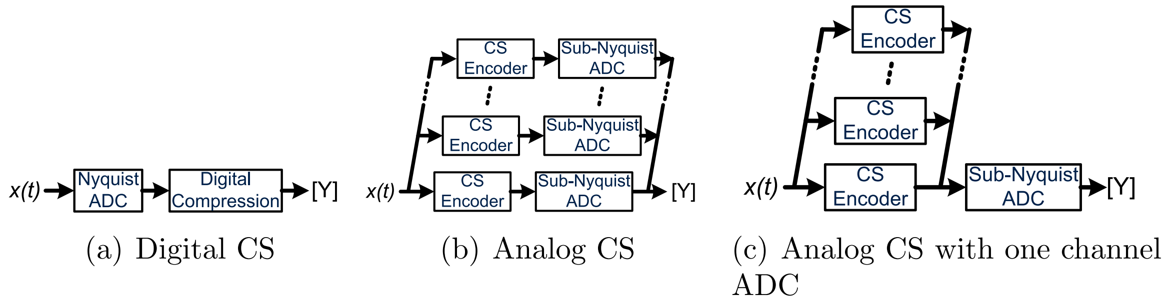

Fig. 1. Block diagram of CS.

$$CR = N/M. \tag{2}$$

For a signal sparse in an arbitrary domain,

$$[X] = [\Psi][\alpha], \tag{3}$$

where $[\Psi]$ is an $N \times N$ sparsifying basis and $[\alpha]$ is the corresponding sparse representation of $[X]$ in the basis $[\Psi]$.

Two factors ensure accurate reconstruction: $[X]$ is sparse in $[\Psi]$, and $[\Psi]$ and $[\Phi]$ are incoherent [8,9,13]. For bio-signal sparse in frequency domain, $[\Psi]$ is an inverse Fourier transform matrix. For ECG signals, an inverse wavelet transform matrix is widely used as $[\Psi]$. The wavelet transformation can be described by a filter bank each containing a high-pass filter and a low-pass filter derived by the 'motherwavelet' [14] (Fig. 2). The decomposition level of the tree structure determines the sparsity of $[\alpha]$. Daubechies wavelets are popularly used as motherwavelets for ECG signals, because their scaling and time dilation approximate typical ECG pulses (i.e. QRS complexes) [4]. Fig. 3 displays the wavelet functions of 4 Daubechies wavelets with different filter lengths. The matrix $[\Psi]$ is determined both by the wavelet decomposition level and the filter length. To choose the optimal motherwavelet, simulations are done to create a maximum sparsity of α by varying the wavelet decomposition level and filter length. The result in Fig. 4 shows that the 'db4' motherwavelet (with filter length 8) achieves the highest percentage of sparsity and furthermore that 5 decomposition levels are enough to get sufficient sparsity. As a result, the best $[\Psi]$ is built by the 'db4' wavelet with 5 decomposition levels. All the ECG signals used in this paper is from the MIT-BIH Arrhythmia Database in PhysioBank [15,16].

In order to obtain high incoherence between $[\Psi]$ and $[\Phi]$, a universal popular choice for the measurement matrix $[\Phi]$ is random matrices, such as (1) a Gaussian distribution; (2) a symmetric Bernoulli distribution. In this paper 1-bit Bernoulli random matrix is applied ($P(\Phi_{i,j} = 1) = 0.5$, $P(\Phi_{i,j} = 0) = 0.5$).

Ideally, $[\hat{X}] = [\Phi]^{-1}[Y]$, where $[\hat{X}]$ is the reconstructed vector. However, as $[\hat{X}]$ has N unknowns and $[Y]$ has only M knowns, $[\Phi]$ is non-square and non-invertible [4]. As a result, optimization methodologies are needed for reconstruction. Table 1 lists all the reconstruction algorithms used in this paper. The details of these algorithms are explained in the researches [17,18].

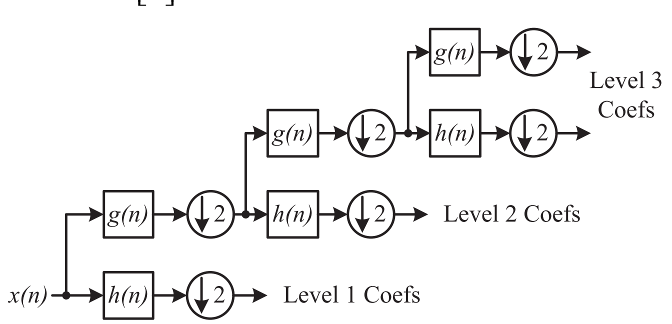

Fig. 2. Three level tree structure for decomposed wavelet coefficients.

3. System design

Based on the theoretical analysis before, the proposed analog CS encoder is designed as shown in Fig. 5. A 1-bit random matrix $[\Phi]$ is generated by a random matrix generator and multiplied with the input analog signal by 64 channels of Multiplying Digital-to-Analog Converter/Integrators (MDAC/Is). The products are integrated at the output of the MDAC/Is, where the compressed output vector $[Y]$ is generated. Instead of 64 parallel SAR-ADCs, a multiplexer, with which only one SAR-ADC is utilized, is employed. The SAR-ADC can be turned off during the $[Y]$ calculation phase of the MDAC/Is. As a result, the power of the ADC can be significantly reduced.

3.1. System consideration

As typical ECG signals has bandwidth of 100 Hz, common ECG systems use 250 Hz as the sampling frequency, which is also applied as the clock frequency of the proposed MDAC/Is. 64 channels of MDAC/Is generate 64 vector elements of $[Y]$. In order to get $CR=2$, the matrix $[\Phi]$ should have a size of 64×128, which means that in every period, 512 ms of the ECG signal is multiplied with ϕ_i to obtain $[Y]$. The ADC should finish the sampling during the final holding time (2 ms) of the output capacitors of the MDAC/Is.

3.2. Random matrix generator

Linear Feedback Shift Registers (LFSRs) are a common pseudo-random sequences dynamical generator. LFSR typically contains a shift register built by D type flip-flops and one or more feedback obtained by exclusive-or (XOR) gates. The initial values ('seed code') of the LFSR have to be loaded in the reset phase. The positions of feedback, which is called 'taps', are chosen based on [19]. The design of the matrix generator is based on the 128-bit Fibonacci LFSR. The outputs of every odd flip-flop is selected to obtain 64 random sequences. The clock frequency of the matrix generator is set to 250 Hz and the reset takes place every 512 ms (or 128 clock cycles).

3.3. MDAC/I

64 MDAC/Is multiply the analog input signal with the digital random sequence and integrate the result. The operation frequency is the same as the matrix generator ($f = 250$ Hz). Fig. 6 describes the architecture of MDAC/I and its operation diagram. In