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Implementation of time-aware sensing technique for multilevel phase change memory cell

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ABSTRACT

This paper introduces and tests a time-aware sensing scheme to overcome the drift issue in Multi-Level Phase Change Memory (MLPCM). Adaptive resistance thresholds are calculated based on statistical data to generate timely reference levels for comparison. Simulations are carried out utilizing MLPCM cell model that mimics the physical behavior of MLPCM cell. The simulation results were then compared against experimental data, and it was noted that simulation results of the used MLPCM model are in close agreement with the experimental data. Furthermore, the time aware sensing scheme provided an accurate reading of the stored bit values given that the timely reference levels successfully compensated for the drift phenomenon. Finally, an application of time aware sensing coupled with MLPCM was implemented, where MPLCM is used as memory element in a Look Up Table (LUT). The suggested MLPCM based LUT utilizes the density and reliability offered by MLPCM paired with the presented time aware sensing scheme.

1. Introduction

Phase Change Memory (PCM) is an emerging non-volatile resistive memory technology that offers low power consumption, high switching and operating speed, long data retention, and high density [1] through its multilevel operation feature. Each cell can be programmed up to 2^N resistance levels and store N bits. Multi-Level Phase Change Memory (MLPCM) is essential for PCM to fulfill its complete potential as storage class memory, and its competitiveness in the market [2]. MLPCM has been recently implemented [3] however; experimental results suggest that time-dependent resistance drift, thermal disturbance and noise [2] in PCM are critical reliability issues that can cause severe data loss [4].

A physical model that assesses the drift phenomenon can help in mitigating the resulting reliability drawbacks in multilevel operation. When intermediate resistance levels and neighboring levels overlap and jeopardize the accuracy of the readout of all programmed states [4]. This paper considers the drift phenomenon, taking into account the difference in drift exponents corresponding to different resistance levels for the same cell; resulting in more accurate drift forecast.

The paper reviews previous works aiming to minimize the drift effect in MLPCM. Then presents a time-aware sensing scheme to mitigate drift caused errors; where an adaptive reference resistance based on statistical data of drift is generated for more accurate readout process. Finally, the use of MLPCM as memory element in Look Up Table (LUT) of Field Programmable Gate Array (FPGA) was explored. It was found that drift restricts the density advantage MLPCM offers. However, the use of time aware sensing allows full utilization of MLPCM capabilities as LUT memory element.

The layout of the rest of this paper is as follows; Section 2 presents background about PCM programming and multilevel programming methods, an explanation of the origin of the drift phenomenon, a review of PCM models, and review of related previous work on drift mitigation. Section 3 explains the proposed time-aware sensing scheme. Section 4 displays the simulation results and compares them to experimental data. And in Section 5 MLPCM based LUT example is presented, while the paper is concluded in Section 6.

2. Background

2.1. PCM operation & multilevel programming

Data storage in MLPCM depends on the thermally induced phase change property in Chalcogenides ($Ge_2Sb_2Te_5$(GST) in this work) utilizing Joule heat effect. The material can exist in highly resistive amorphous, low resistive crystalline and intermediate resistance levels that can be described as crystallites embedded in a bulk of amorphous material [5]. With each programmed resistance level representing a binary equivalent.

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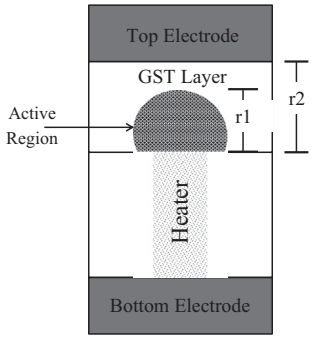

Fig. 1. Cross section of PCM cell mushroom structure (r1 = 50 nm, r2 = 100 nm).

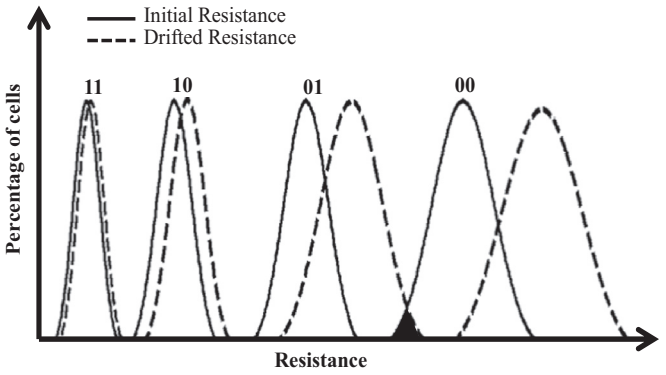

Fig. 2. Initial programmed and drifted resistance distribution at different PCM resistance levels.

The structure of PCM cell used in this work is referred to as mushroom cell as shown in Fig. 1. In this structure the phase change material layer is sandwiched between two electrodes. The thickness of the layer used in this work is 100 nm as shown in Fig. 1. However, in terms of scaling the material volume; no fundamental limitations of phase change and electrical properties were exhibited. And amorphous nanoparticles were experimentally found to be stable in amorphous states at room temperature [6,7].

Multilevel operation is achieved by programming the phase change material into intermediate states between the two corner (fully crystalline and fully amorphous) states. To program into intermediate levels two general methods are used; partial crystallization or partial amorphization. In the former method, the intermediate levels are reached by crystalizing a fully amorphous volume with varying pulse durations. Given that the crystalline part is actually percolation paths that increase in diameter with longer pulses. Thus, pulses with longer durations result in smaller resistances. In the later method a fully crystalline material is partially amorphized by controlling the programming pulse amplitude. Where pulses with higher amplitudes melt amorphous caps with larger radiuses, thus higher resistance [8,9]. The partial crystallization was adopted in this work as the PCM model used [10] supports it. And the crystalline volume is calculated with Johnson-Mehl-Avrami-Kolmogorov (JMAK) equation.

2.2. Drift phenomenon

Drift is a gradual increase noted in amorphous material resistance and threshold voltage. It has been attributed to structural relaxation and stress release in the amorphous material [4]. Drift is physically described as a short-range ordering process where a substantial disorder is still kept on the long range. This reordering is caused by rearrangement at atomistic-level (defect annihilation) of the disordered structure, and change in density of localized states accompanied by an energy release [11,12]. This leads the material to evolve into a thermodynamically stable state. Drift affects the electrical properties of the chalcogenide material i.e. increasing threshold voltage and resistance as shown in Fig. 2. Since the drift process is directly linked to the defects in the amorphous structure after programming, it can be stochastic in nature.

2.3. MLPCM cell model

Phase change memory models are generally composed of interconnected basic modules that simulate the electrical and thermal behavior of a PCM cell. In technical literature there has been many proposed PCM cell models [10,13–22]. The model presented in [13] was successful in generating different resistance levels based on the programming pulse. By calculating temperature and crystalline fraction resulting from that pulse, yet it did not demonstrate the I-V characteristics or the continuous transition of resistance levels. Instead discrete resistance values were modeled with constant resistors. The model in [14] offered a further improvement on the concept of [13] by minimizing the number of circuit elements required in the circuit model on the PCM device. It included multilevel operation where the cell resistance is a function of the duration of the programming pulse. Yet the model has not addressed the drift issue which is an intrinsic phenomenon of the PCM device behavior. The model presented in [15] provided both DC and transient simulations for the PCM device, and succeeded in generating the standard I-V characteristics. However, the model did not provide a thermal simulation nor did it entertain the multilevel operation concept or subsequent drift phenomenon.

Further comparisons of PCM models found in literature are outlined in Table 1. Where the main features desired in the model are addressed, i.e. the model's ability to generate the proper I-V curves at different resistance levels, and accounting for the resistance drift phenomenon. The model in [10] modeled multilevel operation and provided an accurate account of drift in MLPCM. Therefore, [10] was the model used in this work.

A block diagram of the used model [10] is shown in Fig. 3, where the interconnected modules are shown along with the flow of signals between them. The electrical module represents the PCM cell equivalent circuit and is responsible of generating the cell resistive state at all times. Based on that resistance and according to the applied external voltage the thermal module calculates the temperature within the active region. The temperature is then used by the crystalline module that utilizes JMAK equation, to calculate the crystalline ratio in the phase change material layer.

The drift module calculates the drifted parameters i.e. the resistance and threshold voltage, in (1) and (2) based on the empirical laws provided in literature [12].

$$R_{drift}=R_0\left(\frac{t_{off}}{t_0}\right)^{\nu_r} \quad (1)$$

Table 1
Comparison of PCM models.

Model	*I–V* characteristics	Multilevel operation	Drift phenomenon
[10]	✓	✓	✓
[16]	✓	✓	✓
[17]	✓	✗	✗
[18]	✓	✓	✗
[19]	✓	✓	✗
[20]	✓	✓	✗
[21]	✓	✓	✗