Microelectronics Journal 56 (2016) 134–141

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Output capacitor-free low-dropout regulator with fast transient response and ultra small compensation capacitor

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ARTICLE INFO

Article history:
Received 21 September 2015
Received in revised form
27 June 2016
Accepted 22 August 2016

Keywords:
Dynamic biasing technique
Load transient response
Low-dropout regulator
Slew-rate enhancement
Capacitive coupling

ABSTRACT

A output capacitor-free low-dropout regulator (LDO) with fast transient response and ultra-small compensation capacitor is proposed. The slew-rate enhancement (SRE) circuit based on dynamic biasing technique is designed to improve load transient response for 100 mA load step. The SRE circuit structure does not use any passive element to save silicon area and cost. The total active area of the proposed LDO is 0.043 mm^2 with 0.4 pF on-chip compensation capacitor and the stability analysis is also included. The proposed LDO is implemented in 0.35 μm process and experimental results show that it regulates the output voltage at 1.8 V and 1 V with dropout voltage of 200 mV, 100 mA maximum output-load current. The measured quiescent current is 15 μA only. For a 2 V input voltage, the proposed LDO is able to regulate output voltage of 1.8 V within 2 μs with less than 148 mV overshoot and undershoot. For a 1.2 V input voltage, the LDO is able to regulate output voltage of 1 V within 3 μs with less than 152 mV overshoot and undershoot.

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1. Introduction

One type of voltage regulator, a low drop-out (LDO) regulator [1–8,10–14,16–20] is widely used for voltage regulation due to its generality and significance in the IC power management. It is characterized by its low drop-out voltage. Dropout voltage is the minimum difference between the input unregulated voltage to the LDO and the regulated voltage output from the LDO at maximum output-load current. The topology of typical LDO is shown in Fig. 1. The LDO includes an error amplifier (EA), a power transistor (M_P) and resistance network (R_1 and R_2). The error amplifier is connected to the gate of the power transistor. The source of the power transistor is connected to a voltage supply (V_{DD}). The resistance network is connected to the output of the LDO. The node, V_{fb} providing a scaled down version of the output voltage between the resistors R_1 and R_2 is connected to a non-inverting input of the error amplifier where it is compared to a reference voltage (V_{ref}). The amplified error signal is used to maintain the output of the LDO at a predetermined voltage. Therefore, the stability of LDO is one of the challenges in designing LDOs.

In [1,15], the Q-reduction compensation scheme is proposed, it has the advantage of a high phase margin at heavy output-load current, while a pair of complex poles with a higher Q factor is generated at light output-load current and the total value of the on-chip compensation capacitor is 6 pF. In [2], it is achieved with the zero (Z_{ESR}) generated by the equivalent series resistance (R_{ESR}) of the output capacitor (C_{out}), where Z_{ESR} is given by $Z_{ESR} = 1/R_{ESR}C_{out}$. It is generally done by introducing zero in the left-half plane to compensate/cancel the non-dominant pole as long as the non-dominant pole location is fixed. However, the method has inherent problems when driving a variable load. Once the non-dominant pole's location varies, due to the output-load current, power supply, or process, then the fixed zero no longer compensates for the variable non-dominant pole suitably. In [3], to ensure the LDO is stable under different output-load current, the variable compensation structure is implemented using 1-bit programmable capacitor array. The equivalent compensation capacitor is adjusted by sensing the gate voltage of power transistor through non-overlapping phase generator. The total value of the on-chip compensation capacitor is 60 pF. In [4], the proposed power transistor structure mainly utilizes its parasitic gate to drain capacitance and the additional resistors to generate the required pole-zero pairs completing the compensation scheme. However, the total value of the additional resistors is 281 KΩ which occupies a lot of chip area.

During steady-state operation, the magnitude of the output voltage signal is maintained at the predetermined value. If the output-load current changes abruptly and the main regulation loop may not respond quickly because it has a bandwidth limitation. Improving load transient response is the other challenge in

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http://dx.doi.org/10.1016/j.mejo.2016.08.012
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designing LDOs. In [5], the adaptively biasing technique is adopted. As the output-load current increases, the bias current also increases to extend the loop bandwidth, which results in higher power consumption. In [6], a momentarily current-boosting voltage buffer is proposed to provide an extra current to charge and discharge the gate capacitance of the power transistor. In [7], the direct voltage-spike detection makes use of the output-voltage variation to increase the slew rate at the gate terminal of the power transistor momentarily. In [8], the proposed slew-rate enhancement circuit is basically formed by two capacitive-coupling networks to momentarily adjust the gate voltages of charged and discharged transistors for improving load transient response. To ensure good coupling, the value of external-passive elements must be large, which includes a large number of external bulky components, more PCB board space, and higher cost. This goes against the trend which is pushing for higher integration and smaller chip area. In [16], an assistant push-pull output stage using a bootstrap technique is proposed. Due to the high voltage, the thin oxide transistors are needed to implement in this circuit. The cost of this LDO is increased. Beside of this, the delay time and input offset induce in the comparators are need to be taken care. In [17], by using a novel subthreshold slew-rate enhancement (SSE) technique is presented. The proposed circuit needs one output-voltage-detecting capacitor, Ct. The value of Ct is small as 0.4Pf, but which occupies some of the silicon area in the LDO. In [18], the proposed current mode transconductance amplifier (CTA) in which local common-mode feedback (LCMFB) technique is used to enhance the slew rate of the amplifier. Both two resistors R1 and R2 act as a common-mode feedback circuit in the LCMFB. The resistance value and layout of this technique must be carefully designed. Otherwise, the LCMFB will be failed. In [19], the assistant push–pull output stage (APPOS) circuit can improve the transient response time of LDO significantly while only consuming very low bias currents for two complementary current comparators. But the overdrive voltage of comparator's input stage must be carefully designed to prevent the APPOS circuit from being falsely triggered in the steady state or being prematurely turned off before the completion of the transitions. Thus, there is a need for a circuit that improves the transient response of the LDO regulator to avoid the above mentioned constraints. In this work, a low-dropout regulator with fast transient response and ultra-small compensation capacitor is presented. The proposed slew-rate enhancement (SRE) circuit structure does not use any passive element to save silicon area and cost. The organization of this research is given as follows: Section 2 describes the details of the proposed LDO with SRE circuit. Section 3 discusses the stability analysis and simulation results. Section 4 presents experimental results. Finally, the performance summary and the conclusion are drawn in Section 5.

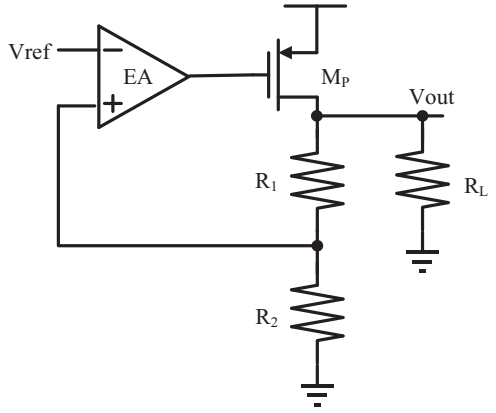

Fig. 1. The topology of typical LDO.

2. The proposed ldo with sre circuit

2.1. Circuit structure

The circuit schematic of the proposed LDO is shown in Fig. 2. The quiescent current distribution when zero load current is indicated in Fig. 2. The folded-cascode amplifier (M_6–M_{14}) is the first stage which is connected with bias circuit (M_1–M_5), non-inverting amplifier (M_{15}–M_{18}) is the second stage. The power transistor (M_P) connects to the output of the second stage is designed to deliver maximum output-load current across a wide-range supply voltage. The on-chip compensation capacitor (C_C) couples between the source terminal of transistor M_{12} and the output terminal Vout of the LDO. The proposed SRE circuit (M_{19}–M_{22}) is designed to improve load transient response of LDO with dynamic biasing technique for the second stage.

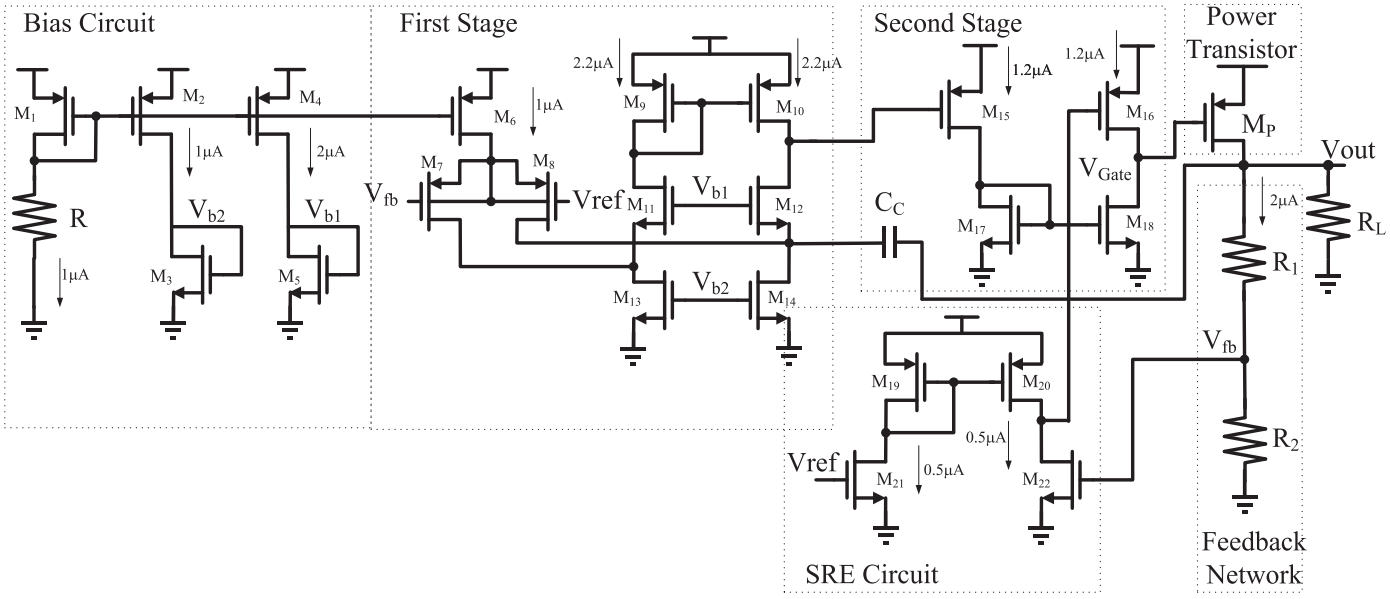

Fig. 2. The circuit schematic of the proposed LDO.

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