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Phase error reduction of a digitally controlled phase shifter utilizing a variable phase and gain amplifier

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ABSTRACT

This paper presents a variable phase and gain amplifier (VPGA), featured in a 4-bit digitally controlled phase shifter, that enables significant phase error reduction. The functionality of the VPGA is demonstrated by utilizing it between the third and fourth bits of a digitally controlled phase shifter. The first three bits are implemented using distributed active switches based on HBTs and the fourth bit is realized in a final amplification stage based on switching between common-base (CB) and common-emitter (CE) topologies. By the use of the VPGA, RMS phase error is reduced from 22° to 11° with the cost of reduced gain (0.1–2.5 dB) and increased RMS gain error (1.0–2.2 dB). A total of 360° phase shift is achieved in 4 bit resolution with an RMS phase error of 0.1° at 10.5 GHz, and a maximum 11° phase error in 4.5 GHz bandwidth. The chip area is 2.150 mm × 1.040 mm including pads, and the VPGA consumes only 0.32 mm × 0.410 mm area. The chip is implemented in a 0.25-μm SiGe BiCMOS process. These performance parameters are attributed to the adjustment method by the VPGA applied in this work, which enables superior performance than the-state-of-the-art utilizing similar technologies.

1. Introduction

Transmit/receive modules are essential parts of modern phased arrays to achieve fast beam scanning and electronic beam control functions. These modules determine overall performance of phased arrays. For T/R modules that are based on the all-RF system architecture, phase shifting is performed at RF frequencies. In these modules, phase shifter (PS) is shared for both receiving and transmitting paths through SPDT switches, requiring no additional bidirectional phase and magnitude control circuit [1]. PS is one of the key components of a T/R module that determines the phase resolution of the system [2]. Recent developments in silicon process technologies have enabled design of Si-based highly compact and low cost phase shifters [3]. Three important design techniques are widely used in phase shifters: switched filter, vector sum and distributed active switches.

In switched filter type phase shifting, the signal path is swapped between two LC based filters that have different phase responses. There exist mainly two ways of creating phase difference between states using this technique; high-pass/low-pass (HP/LP) [4,5], and by-pass/low-pass (BP/LP) [2,5] filter types. Up to 90° phase shift can be obtained in a high-pass or low-pass Π- or T-network. Due to switching between two different filter types, up to 180° phase shift can be obtained. For an HP/LP filter based PS, each phase selection bit requires two SPDTs. Under these conditions, a BP/LP filter based PS can be a good candidate as each phase selection bit can be realized with only a single series switch. However, this type of PS is capable of providing up to 90° phase shift, and in a narrowband operation. Combination of HP/LP and BP/LP type PS are widely used in literature [2,5,6]. However, these types of PS have significant disadvantages. First, due to the lack of very low insertion loss RF switches in Si CMOS or SiGe BiCMOS technologies, high-resolution passive phase shifter topologies have significantly high insertion loss. For a 5-bit phase shifter this loss can be up to 20 dB [6]. In addition, as the resolution of the phase shifter increases, the area consumption also increases.

Recently, respectable amount of research have been done on active phase shifters utilizing the vector-sum method [7–9]. Remarkable phase resolution and higher gain can be achieved in a smaller area in vector-sum architectures compared to passive PS. The fundamental idea of the vector-sum method is to generate the desired phase by combining amplitude modulated in-phase and quadrature vectors. In this type of phase shifters, a poly-phase filter is widely used to generate in-phase and quadrature vectors. These filters have very high insertion loss that is generally compensated with an active balun, leading to a significantly high power consumption.

It is inherently difficult to correct the phase shift errors in the above-mentioned phase shifter topologies after fabrication. This paper presents the utilization of a VPGA in a 4-bit digitally

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controlled phase shifter that enables the adjustment of the phase shifts. This technique is applied on a phase shifter based on distributed active switches, featuring high gain, low power consumption and reasonable phase error. The circuit is fabricated in a 0.25 μm SiGe BiCMOS technology. The novelty lies in the utilization of the VPGA to adjust the phases and reduce the RMS phase error with a slight cost of additional RMS gain error and lower average gain. A cascode amplifier with an R-C feedback is used as the VPGA, and designed to exhibit maximum phase variation across its control voltage range. Both in the VPGA and the phase shifter, npn-HBTs are used in order to decrease the number of cascaded amplifier stages and power consumption. Section two explains the circuit design aspects and section three discusses simulation and measurement results.

2. Circuit design

The distributed amplifier technique is applied in the design of the first three bits [3]. L–C ladder stages are used for phase shifting and eight stages are cascaded. Each L–C ladder stage is connected to a cascode amplifier. The bias voltage of the cascode transistor is used to select the desired phase state. The fourth bit is a 180° phase shifter based on switching between common base (CB) and common emitter (CE) amplifiers. CE and CB amplifiers are connected to the same node, and current flow of amplifiers is controlled to provide the required phase shift.

Fig. 1a shows the phase shifter topology consisting of cascaded ladder networks with series inductor (L) and shunt capacitor (C). The number of LC stages determine the resolution of the phase shifter. For such LC ladder based phase shifters, the optimum number of stages is around eight. Higher number of stages do not provide sufficient RMS phase error improvement to overcome the increased area consumption and insertion loss [3]. Using eight stages, a total of 180° phase shift is obtained in 3-bit resolution; and including the final 180° bit, a 4-bit phase shifter is obtained. The phase shift per section is given by $\Delta\varphi \approx \omega\sqrt{LC}$, [10]. L and C values are optimized to provide 22.5° phase shift at 10 GHz for each stage separately, since each stage introduces slightly different parasitics due to the asymmetrical layout. This phase shift is proportional to the operating frequency, so the phase error increases for wide bandwidths. To obtain a desired phase shift, the appropriate HBT cascode pair is selected by applying proper bias voltages, whereas the bias voltages of the other seven cascode pairs are set to GND.

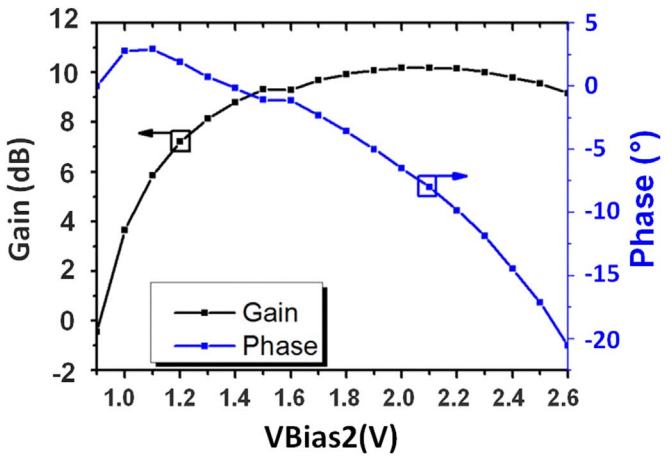

Fig. 2. Phase control with VPGA and gain variation. If V_{bias2} is kept between 1.4 V and 2.6 V gain variation is less than 1 dB.

Fig. 1b shows the schematic of the VPGA that is designed to compensate the RMS phase error of the first stage resulting mainly from inductive coupling. One way to compensate these phase errors is to use a MOS based varactor. However, its quality factor degrades as frequency increases, which introduces more insertion loss and gain error [11]. Instead, in the proposed VPGA, the base-emitter junction capacitance of Q3 is used for this purpose. The voltage Vbias2 is applied to Q3 over a resistor, in order to control its junction capacitance, CbeQ3. Referring to (1), the additional phase shift that is introduced by CbeQ3 and Lp2 is controlled by Vbias2. This bias voltage is used to adjust the capacitance and compensate the phase error. Additionally, an R–C feedback is used in order to increase the bandwidth of the amplifier for better matching, at the cost of slightly lower gain. Fig. 2 shows the gain and phase of the VPGA as a function of control voltage at 10 GHz. If Vbias2 is controlled within the region of 1.4–2.6 V, gain variation is less than 1 dB and phase control range is around 20°, which is sufficient to reduce the phase error of the whole phase shifter in Fig. 1a. In order to improve the phase error performance of the phase shifter, the frequency spectrum is divided into three bands, in which three different bias configurations are applied for adjustment purposes. The relative phase difference varies with frequency; therefore, the circuit is optimized to provide minimum phase error at three center frequencies (at 8.75, 10.25, and 11.75 GHz) for three modes. Depending upon the operation frequency, one of the three sets of bias voltages is selected and the

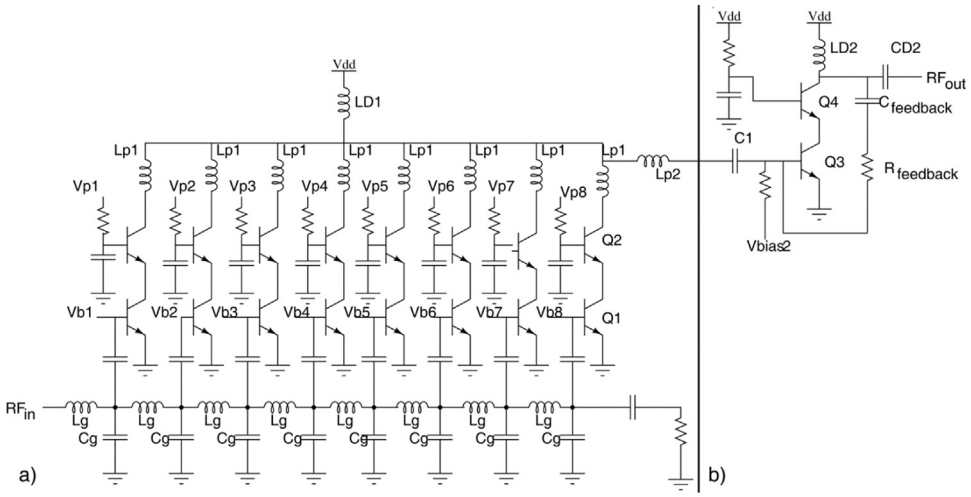

Fig. 1. a) Schematic of the BiCMOS phase shifter using distributed active switches, b) schematic of VPGA.