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An analog circuit synthesis tool based on efficient and reliable yield estimation

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ABSTRACT

Analog circuit design has become a very challenging and time consuming process for circuit designers due to increased non-idealities and worsening variability phenomena. In order to facilitate the design process, several analog circuit sizing tools have been proposed in the literature. These tools have then led to yield-aware ones, where a certain yield is targeted. However, the type of variability analysis to be employed is still a topic of discussion due to the challenging trade-off between accuracy and efficiency of the yield analysis. Quasi-Monte Carlo (QMC) approach is one of the efficient techniques that provides efficient variability analysis via deterministic, and more importantly homogeneous sampling. The major bottleneck of the conventional QMC is that there is no practical way to calculate the estimation error. Scrambled-QMC has been utilized to obtain the error bounds of the estimation, thanks to multiple runs of randomized sample sets. However, the requirement of multiple runs substantially increases the synthesis time. To overcome this problem, this paper proposes a novel yield-aware analog circuit sizing tool, where an adaptive sample sizing algorithm for scrambled-QMC is employed in the yield estimation part.

1. Introduction

Mixed-signal designs occupy a large fraction of recent integrated circuits. The design of the digital section of the IC has been fully automated with powerful digital circuit synthesis tools. However, mixed signal ICs also need an interface to communicate with the continuous-valued world, where analog sections meet this requirement [1]. The case of analog synthesis is quite problematic due to the requirement of comprehensive analyses for the complicated trade-offs among various aspects of performances. Furthermore, as a result of scaling differences between transistor dimensions and process tolerances in sub-micron technologies, variations in different fabrication steps are drastically increased, which alternate the device parameters significantly [2,3]. As a result, a discrepancy occurs between the expected and the actual performances in a population of manufactured ICs [4,5]. Therefore, analog circuit design has become a more challenging problem for circuit designers, who follow the conventional flow described in Fig. 1. However, in practice, variability analysis is included in the flow, where parameter variations are considered in order to be able to guarantee a certain yield after the production. This variability loop is repeated and circuit sizing may be re-called many times until a robust solution is obtained. At the end, the main loop is finalized by designing the layout for a solution that satisfies both electrical and yield constraints. However, considering these analyses and numerous sizing iterations, the overall design time increases, which degrades the time-to-market of an integrated circuit.

To overcome this problem, several automated sizing tools [6–12] have been proposed over the last two decades. Even though automation of the analog sizing part improves the design time, expensive yield analysis still limits the total synthesis time. One solution may be performing yield analysis only for candidates satisfying all electrical design constraints. However, in this case, the trade-off between electrical specifications and the yield is ignored, and solutions having quite acceptable electrical performances with higher yield may be overlooked. Infeasible solution elimination (ISE) [13,14] have been proposed in order to deal with this problem. However, efficient yield estimation techniques are still a subject of great interest to enhance the efficiency of yield-aware circuit sizing tools.

Conventionally, sensitivity-based analysis [15,16], worst case (corner) analysis [17–19], response surface models (RSM) [20–22], and Monte Carlo (MC) based analysis have been commonly used for variability analysis [23–25]. Among all of these methodologies, MC-based approaches are commonly preferred thanks to the ease of use and quite accuracy. However, the primitive MC approach

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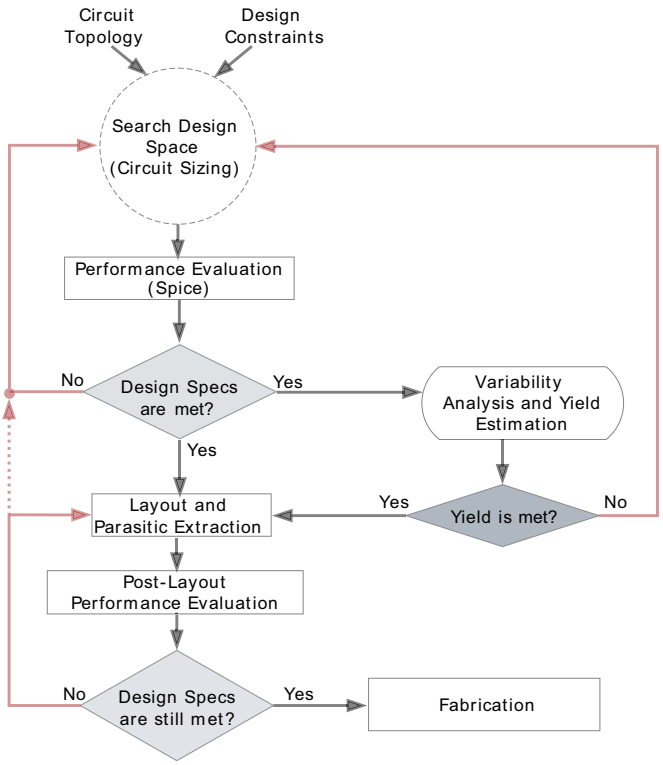

Fig. 1. Conventional analog circuit design flow and variability aware circuit design.

requires a large number of simulations to provide a certain accuracy, which increases the computational effort. To overcome this inefficiency problem, several speed-up techniques have been developed, such as Latin hypercube sampling (LHS) and Quasi-Monte Carlo (QMC). The idea behind these techniques is to sample the design space intelligently to make accurate estimations with fewer samples. Both approaches are commonly used for a number of different applications including low and high dimensional problems. However, there is not any absolute agreement on which approach is superior than the other. A further discussion can be found in [24,26]. One more important advantage of QMC exhibits itself for applications that require iterative analysis, such as yield-aware optimization. Since QMC is a deterministic approach, the sample size can be increased iteratively. In [14], an adaptive sample sizing algorithm for the QMC approach was introduced and discussed for yield-aware optimization. On the other hand, the major disadvantage of the conventional QMC is that the error of the estimated yield cannot be determined in any practical way. To overcome this issue, QMC is randomized by reordering of the samples (scrambling) [27]. Thus, an artificial distribution is created and error bounds can be obtained, maintaining deterministic property of each scrambled sample set in itself. In [28], conventional QMC and scrambled-QMC techniques are employed together for yield and confidence interval estimation during yield-aware optimization. To sum up, scrambled QMC-based yield analysis is quite accurate and efficient to be used for yield-aware analog circuit sizing tools. Furthermore, adaptive sample sizing moves the efficiency one step further. In the light of these previous works, this study proposes:

- a comprehensive analysis and discussion on variability analysis and yield estimation with a focus on analog circuit design automation tools,
- a novel yield-aware automation tool including an efficient and reliable yield estimation part, where an adaptive sizing algorithm and scrambled QMC are combined,
- more realistic variability simulations and yield estimation using both inter-die and intra-die variation models that were obtained through fitting measured silicon data.

The reminder of the paper is organized as follows. Characterization results of the test chip for the process variation parameters are provided in Section 2. The proposed approach is introduced in Section 3 and explained in detail in the following subsections. Synthesis examples are provided, and results are discussed in Section 4. Finally, Section 5 concludes this study, providing general remarks.

2. Characterization of process variation effects

Process variations are typically divided into two components: inter-die and intra-die, where inter-die process variations are random in nature, intra-die variations typically exhibit spatial correlations. According to the well-known Pelgrom model given in (1), intra-die variations are inversely proportional to the device area, where $A_{\Delta D_p}$ is the corresponding technology dependent coefficient of parameter D_p. Conventionally, variations in threshold voltage, oxide thickness, transistor length and width are considered during the variability simulations.

$$\sigma_{\Delta D_p} = \frac{A_{\Delta D_p}}{\sqrt{W \cdot L}} \tag{1}$$

A characterization chip shown in Fig. 2 was designed, manufactured, and measured to obtain both inter-die and intra-die variation variables for the used technology. There are mainly 4 different blocks resided within the same chip, where each sub-block includes 64 independent transistors (32 n-type + 32 p-type) with different W/L ratios. Control units A and B provide individually addressing of each single transistor, which multiplex the