Pilot assisted readout for passive memristor crossbars

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ABSTRACT

The high demands for performance and energy efficiency pose significant challenges for computational systems. Memristor-based crossbar architectures are actively considered as vital rivals for the traditional solutions. Nonetheless, density and energy driven passive array structures, that lack a switching control per cell, suffer from sneak paths that limit the range of accurate operation of the crossbar array. In this paper, the crossbar array is treated as a communication channel with added distortion to represent the sneak current. Estimation techniques based on preset pilots are utilized to alleviate the distorting effects and enhance the system throughput. A two dimensional setting of these reference points leads to an accurate estimation of and compensation for the sneak paths effects. Thereby a comprehensive technique is presented that boosts the performance and accommodates functional metrics of speed, energy efficiency, accuracy and density all within a single envelope. SPICE simulations cover the data patterns dependencies, the non-linearity impact, and the crossbar distortion. It offers a further validation, from several aspects, on the reliable operation attained with the complete separation of the high and low bits regions.

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1. Introduction

Design and technology innovation of computational architectures, along with data and server growth, pose an exigent need for novel approaches. It has initiated a mandated exploration of emerging technologies [1,2] that addresses the set conventions beyond Moore's law [3]. The discrepancy, in the data rate and throughput, between the memory and the processing block stresses further the communication bottleneck; where the memory falls short in providing the anticipated data rates. [4]. Moreover, the extensive scaling has pushed the conventional memory technologies up to its limit, which compromises the main functionality metrics of reliability, speed, and retention capabilities [5].

Memristors are promising candidates that could be up to the stringent challenges in diverse applications [6–11]. The crossbar structure is of particular interest, due to its many advantages, whether in terms of density, efficiency of fabrication and power consumption [12,13]. It has paved its way into memory applications [14–19], including associative memories [20] in the process to bridge the gap between memory and designated computational blocks. It was also adopted in unconventional computing systems, showing high potential for embedded architectures and co-localized in memory computation [21–25]. Neuromorphic processing techniques incorporated the crossbar as well in terms of synapses to overcome the density and integration challenges faced by the current CMOS approaches [26–29].

Data is saved within the memristor-based memory array in the form of resistances. The two memristor boundaries of R_{off} and R_{on} correspond to the bit '0' and '1' respectively. Writing to the memory is accomplished through applying a voltage across the memristor to ensure its switching to either high or low resistance states. While reading out data from the memory requires activating the corresponding row and column of a target cell at a voltage lower than its switching threshold. This density driven adoption of a passive topology, where no access control [6] is available per cell, imposes an additional challenge to be addressed in the read operation; the sneak path phenomenon [6,30,31]. Sneak paths are considered as added distortion to the actual cell data. The read out value of a particular cell is the combination of the saved data along with the added distortion as depicted in Fig. 1a. The sneak paths are a result of having open access to any of the cells in the array. Such circuit structure is adopted in order to preserve the density attained with the memristor crossbar structure. Nonetheless, the presence of sneak paths leads to a large overlap in the regions for the readout values of '1' and '0' bits as shown in Fig. 1b.

A trivial solution to the sneak path problem is to add a switch per cell to control the access, thus leading to gated or 1T1M/1D1M architectures [32,33]. The added switch provides higher reliability but at the expense of increased area per cell and consequently reduced density. Gateless solutions that address the distortion imposed by the sneak path are split into circuit-based and data analysis approaches. The former applies different contexts of architectural [16,34–39] and delay accommodation techniques [17], which achieve improved margins and accuracy of the read-out

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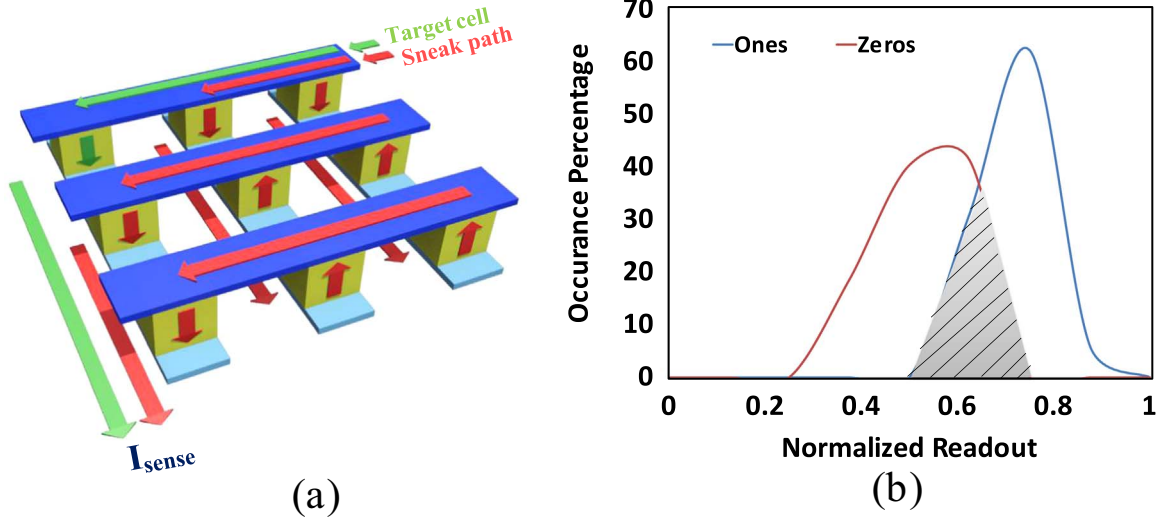
Fig. 1. Sneak Path Origins and Impact (a) Sneak current phenomenon where the sense current is a combination of the target cell value with an additional sneak path current. (b) Distributions for the high and low bits for the readout operation. The histograms are overlapping as a result of the added distortion leading thus to an erroneous detection process.

data while sacrificing other metrics of power efficiency, density and speed respectively. On the other hand, data analysis approaches take the data dependent characteristics into consideration and dampen the sneak current effects by applying information theoretic and statistical principles. These data-constrained measures add complexity to the sensing circuit design [40] and limit the amount of information that could be encoded within the array [17,41,42]. A compromise is encountered in the aforementioned techniques for overcoming the sneak path or distortion limitation. Gated approaches suffer mainly from density limitation but preserves the reliability of operation. On the other hand, gateless approaches prioritize the density measure over all other metrics. Thus, contrasting measures of energy efficiency, circuit design complexity, information constraints, speed, and accuracy are all set forward without a comprehensive solution.

In this paper, we propose a novel readout technique that preserves the advantages of the crossbar array while adhering to the strict design requirements of integration and operation efficiency. We model the sneak path distortion affecting a memory cell as an additive noise that is correlated with the distortion imposed upon the cells in the same row and column. Exploiting this correlation, we devise a technique for estimating the sneak path current by making use of pilots; memory cells that contain known data values. Once the distorting sneak path effect is estimated, its effect can be alleviated. A simple threshold-based readout mechanism can then be employed, and is shown to yield high accuracy. Using SPICE simulations, we demonstrate the improvements achieved in terms of read margins and the resulting complete separation between the high and low bit regions. The simulation setup incorporated the array non-idealities such as the wire resistance. Tests addressed the non-linearity effects, the probability of '1' or low resistance within the array data, and different data patterns including random and NIST memory images [43]. We report the SPICE simulation results for large arrays of 256 kb and reaching up to 1 Mb in size. Incorporating pilots within gateless crossbar arrays could be used for different purposes. At one end, it provides insight to the sneak path and a way to alleviate its effect using a simple linear model. The model is not strictly confined to memristor cells, but is also applicable to other emerging technologies within a crossbar structure. On the other hand, it could also serve as post silicon validation techniques to ensure the operations are within the set constraints.

The remainder of the paper is arranged as follows. Section 2 presents the sneak path model within passive arrays and its estimation principles. The integration of the pilot within the crossbar array and its consequent effect on operation are illustrated in Section 3. Simulations and results of the pilot-assisted readout operation covering different aspects of the data effects and circuit design are discussed further in Section 4. The Discussion in Section 5 holds the analysis of our proposed technique and the comparison with alternative approaches that target the sneak path phenomenon. Section 6 presents the conclusions drawn and a summary of the overall paper.

2. Dynamic sneak path estimation

Reading a cell value within a memory array is usually done through applying a read voltage across the corresponding word line and bit line of the target cell. This approach to the reading operation, with leaving the remaining rows and columns of the memory array floating, comprise a floating rows and columns scheme (FRC). In gateless architectures, the memory cell would be solely composed of the memristor element as a storage device as shown in Fig. 2. The memristor model used throughout the paper is the HP device reported in [17] with equation

$$I = k_{on/off} \sinh(aV) \tag{1}$$

where a and $k_{on/off}$ are 3 V^{-1} and $10^{-9}/10^{-12}$ respectively. Upon activating a particular row and column for the read operation, no cell selector is available to suppress the access to the remaining cells in the memory array. Consequently, current sneaks over to the other cells and forms a significant amount of distortion. The sensed current is then composed of the original cell data along with the sneak path current. Fig. 1a shows a sample of the sneak path current that is added to the target cell to form the readout value.

2.1. Channel model

As current sensing is used in order to read the memory cell value, the sneak paths act as a resistor in parallel with the target cell [6,38]. Thus, the sensed current I_{sense} is the sum of the current of the target cell I_t and the sneak path current I_{sneak}.

$$I_{sense} = I_t + I_{sneak} \tag{2}$$

The sneak current is primarily a function of the complete array