Microelectronics Journal 54 (2016) 72–84

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Electronic frequency compensation of AlN-on-Si MEMS reference oscillators

Ali Kourani [a], Emad Hegazi [b,*], Yehea Ismail [a]

[a] Center for Nano-electronics & Devices, American University in Cairo & Zewail City for Science and Technology, Cairo, Egypt
[b] Integrated Circuits Lab, Ain Shams University, Cairo, Egypt

ARTICLE INFO

Article history:
Received 30 April 2015
Received in revised form
4 April 2016
Accepted 12 April 2016

Keywords:
4G
Wireless
Temperature compensation
Frequency compensation
Phase noise
MEMS
TCXO
Piezoelectric resonator
Reference oscillator
Sigma delta ADC
Phase locked loop
Temperature to digital converter
Incremental ADC
Temperature sensor

ABSTRACT

In this paper we report on the design of a frequency compensation system for AlN-on-Si MEMS reference oscillator to replace temperature compensated crystal oscillators (TCXOs) in cellular handsets. A 76.8 MHz, 105 ppm Temperature Stable, AlN-on-Si MEMS Oscillator is designed to demonstrate the frequency compensation scheme. Double layers of SiO_2 are used for passive temperature compensation. The oscillator consumes 850 μA, with phase noise of −127 dBc/Hz at 1 kHz frequency offset. Temperature drift errors and initial frequency offset of ±8000 ppm are combined and further tackled electronically. A simple digital compensation circuitry generates a compensation word to a 21-bit MASH 1-1-1 $\Delta\Sigma$ modulator included in LTE fractional N-PLL for frequency compensation. Temperature is sensed using 4.6 μA, 11.5 bit temperature to digital converter TDC with resolution of 0.1 °C in 100 ms conversion time. The paper presents the first AlN-on-Si oscillator platform with ±0.5 ppm frequency stability over temperature ranges from −40 °C to 85 °C. The system runs on 1.8 V supply in 32 nm CMOS.

1. Introduction

AT-cut quartz has been the de facto choice for low power frequency references in cellular handsets for decades. First order temperature compensated quartz resonators can result in a frequency stability of ±10 ppm over the commercial temperature ranges from −40 °C to 85 °C, moreover the high quality factor Q and tens of ohms motional arm resistance ensure low power, and low phase noise reference source.

Modern transceiver platforms employ multiple reference oscillators to serve the multitude of services supported. This accelerates the efforts to replace bulky filters and the traditionally-quartz oscillators with MEMS alternatives; pressured by cost and form factor reduction requirements.

MEMS resonators had successfully replaced quartz in markets such as cameras, real time clocking [1,2], and FPGAs. However they are still short of meeting the demanding cellular market with its stringent phase noise, frequency and temperature stability specifications [3–6]. The main hurdle for MEMS resonators in cellular platforms is the sensitivity of resonance frequency to temperature shifts. To quantify, a temperature sensitivity of −31 ppm/ °C, leads to a deviation of 4000 ppm over the full range from −40 °C to 85 °C [6]. Moreover, fabrication tolerance leads to initial frequency offset up to ±8000 ppm [5]; these errors are not tolerable in cellular communications. Silicon based MEMS reference oscillators attained state-of-the-art frequency stability for non-ovenized implementations being reported at ±0.5 ppm [6], ±3 ppm [2]; however the design presented in [2] could not satisfy the LTE phase noise requirements due to the high motional resistance R_m of 90 kΩ and the inferior mechanical coupling which resulted in high phase noise floor. On the other hand, the frequency stability for ovenized MEMS oscillator has been reported at ±0.05 ppm [7], but without addressing the correction of initial frequency offset and fabrication tolerances. Piezoelectric-on-silicon oscillators previously reported frequency stability of ±10 ppm [1] and ±35 ppm [8] which are not suitable for LTE communications requiring <1 ppm frequency stability over −40 °C to 85 °C

* Corresponding author.
E-mail addresses: ali_kourani@aucegypt.edu (A. Kourani), emad.hegazi@eng.asu.edu.eg (E. Hegazi).

http://dx.doi.org/10.1016/j.mejo.2016.04.010
0026-2692/

temperature ranges [9].

In this paper, we extend our previous work [10,11] and propose the first AlN-on-Si MEMS reference oscillator platform with frequency stability of ±0.5 ppm across the temperature range from −40 °C to 85 °C. The proposed design improves the stability by 2 orders of magnitude. The design supports the stringent phase noise LTE specifications; hence, enhances the-state-of-the-art frequency stability performance for non-ovenized devices by over an order of magnitude. Additionally, the paper addresses fabrication tolerances correction. To obtain such improvement the design combines both material [10,11] and electronic compensation with the usage of high Q, small motional resistance AlN-on-Si resonators.

Material compensation incorporates a positive temperature coefficient of frequency TCF material such as SiO_2 in the resonator stack to neutralize the negative TCF of silicon at resonance frequency. Although this method does not consume power, near-zero TCF resonators need thick layers of SiO_2 that negatively impact oscillator's phase noise performance by reducing the resonator's Q and power handling [8,11]. New techniques have been reported to circumvent this issue in [12]. Furthermore, a new generation of silicon devices achieve low temperature dependence without the need for material compensation is reported in [13]. On the other hand, electronic compensation has minimal impact on resonator's Q but is incapable of supporting the needed tuning range (> 1000 ppm) [8] using known tuning mechanisms. Therefore, complete frequency compensation is achieved by combination of both material and electronic compensation.

Temperature drift is corrected by two ways, using SiO_2 as compensating material (reduces drift from 4000 ppm to 105 ppm) [10,11] and low power electronic compensation that additionally reduces initial frequency offset (±8000 ppm) to reach ±0.5 ppm frequency stability over ranges −40 °C to 85 °C. This paper concentrates on the design of electronic frequency compensation system for AlN-on-Si oscillators targeting LTE specifications. 11.5 bit, 0.1 °C resolution temperature to digital converter TDC senses the resonator's temperature using bandgap reference front end with a maximum output error of 0.375 °C. Output frequency is corrected through the high resolution phase locked loop PLL; where, a simple digital compensation circuitry feeds a frequency compensated digital word to MASH 1-1-1 sigma delta ΣΔ modulator controlling the PLL division ratio.

The overall system shown in Fig. 1 consists of a resonator, an oscillator sustaining circuit, a temperature sensor, frequency compensation circuitry and a fractional-N synthesizer. The output of the sustaining circuit is 76.8 MHz reference frequency, which is halved to 38.4 MHz and then fed into a PLL to produce any frequency between 699 MHz and 3590 MHz (LTE bands) with maximum jitter value of 0.826 ps, and minimum of 0.28 ps.

The paper is divided as follows, Section 2 demonstrates the MEMS oscillator design, Section 3 presents the temperature to digital converter, Section 4 is concerned with the electronic compensation system, Section 5 discusses the results and finally Section 6 concludes the paper.

2. MEMS oscillator design

2.1. Resonator design

Energy loss mechanisms limiting the resonator's quality factor Q can be air damping Q_{air}, anchor losses Q_{anc} and intrinsic material losses Q_{MAT} [14]; where, material losses are mainly phonon-phonon losses [15], thermoelastic damping *TED* [16] and phonon-electron losses. The resonator is designed in vacuum; thus, air damping is minimized. The total theoretical unloaded Q is given in

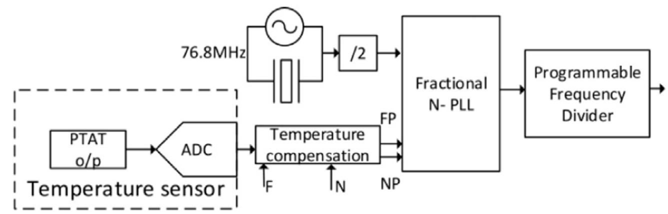

Fig. 1. MEMS oscillator platform.

(1). Akhieser *AKE* phonon–phonon damping is the most dominant loss for MHz range resonators [15]. Analytical modeling and numerical simulations of MEMS resonators can be found in [17,18].

Anchor losses [14] are modeled using perfectly matched layer *PML* in COMSOL. Quarter wave λ/4 anchors [11] of length 35 µm and width 10 µm are used. Fig. 2 shows top view and a cross section from the resonator. Applying AC voltage across the thin *AlN* film induces in-plane vibrations through the piezoelectric d_{31} coefficient, and excites the resonator in the width extensional mode [14]. Finite element simulations showed that Q_{Total} is 9950 [11].

$$\frac{1}{unloaded\ Q_{total}} = \frac{1}{Q_{air}} + \frac{1}{Q_{anc}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{phonon-phonon}} + \frac{1}{Q_{phonon-electron}} \quad (1)$$

Temperature stability [1–11] is a key issue for reference frequency sources. Poor temperature stability causes activity dips which results in loss of GPS lock, dropped packets and cellular signal error. SiO_2's positive TCF compensates for silicon's negative TCF. The resonator achieves temperature stability of 105 ppm instead of 4000 ppm for the uncompensated resonator over temperature ranges −40 °C to 85 °C as shown in Fig. 3 [11]. Resonator's Butterworth Van Dyke BVD model [14] is shown in Fig. 4a, while the resonator's input impedance is shown in Fig. 4b; 125 Ω motional resistance resonator is designed for low power oscillator [11].

2.2. Oscillator design

As the size of the resonator shrinks, Q near the parallel resonance becomes poor due to smaller C_f and C_p capacitances that parallel resonate with L_m. Series resonance Q is less sensitive to resonator's size shrinkage since it is less affected by device parasitics. Working around series resonance rather than parallel resonance (as in quartz) preserves the loaded Q and maintains phase noise performance [11,19]. Small amount of pulling from the mechanical resonant frequency is needed to minimize the frequency dependence on electrical parameters, thus improving the oscillator's frequency stability. Pulling value P_c at critical condition for oscillation is given in (2) [20]. The series resonant oscillator consumes less power ($\alpha 1/P_c$) than the parallel resonant one ($\alpha 1/P_c^2$) for the same pulling value, making it more suitable for cellular phone platforms. Series resonance oscillator is shown in Fig. 5. The small signal loop gain [19] is given in (3); where, Z_s is the resonator impedance, and C_s=$C_p/2$

$$P_c = -\frac{C_m}{2C_s}(\omega C_L R_L)^2 \quad (2)$$

$$\text{Gain} \approx \left(\frac{g_m(R_L/2 \| 2C_L)}{1 + g_m(Z_s \| C_s)/2}\right)^2 \quad (3)$$

Superior phase noise floor is achieved through carefully designed duty cycle corrector and inverter buffers for the smallest rise and fall time durations, which is enhanced using 32 nm kit technology [11]. Oscillator's phase noise profile across PVT is shown in Fig. 6. The worst results are in the minimum gain corner: