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Analysis of propagation delay and repeater insertion in single-walled carbon nanotube bundle interconnects

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ABSTRACT

A new closed-form expression of 50% propagation delay for distributed *RLC* interconnects is proposed using the multivariable curve fitting method, with a maximum error of 4% with respect to SPICE results. Then accurate closed-form solutions for the optimum repeater number and size to minimize the propagation delay are further derived. The performance of single-walled carbon nanotube (SWCNT) bundle interconnects is evaluated using the proposed models in the intermediate and global levels at the 22- and 32-nm technology nodes, and compared against traditional Cu interconnects. It is shown that the performance of SWCNT bundle interconnects in propagation delay can outperform Cu interconnects, and the improvement will be enhanced with technology scaling and wire length increasing. On the other hand, the propagation delay of SWCNT bundle interconnects is super-linearly dependent on the wire length similar to Cu interconnects, indicating that the method of repeater insertion to reduce the propagation delay can also apply to SWCNT bundle interconnects. The results shown that repeater insertion can really reduce the propagation delay of SWCNT bundle interconnects effectively, and the optimum repeater number is much smaller than that of Cu interconnects.

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1. Introduction

With technology scaling, the propagation delay of interconnects has become one of the key factors restricting the overall performance of gigascale integration [1]. As the lateral dimensions into the nanometer scale, the resistivity of traditional Cu interconnects will increases significantly, which will seriously degrade its delay performance. In recent years, due to their extremely desirable properties of high mechanical and thermal stability, high thermal and electrical conductivity and large current carrying capacity, carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) have aroused a lot of research interest [2,3]. However, GNRs are beyond the scope of this paper. CNTs can be classified as single-walled CNTs (SWCNT) with only one shell and multi-walled CNTs (MWCNT) with several concentric shells. The high intrinsic ballistic resistance of approximately 6.45 kΩ associated with an isolated SWCNT suggests the use of bundles consisting of numerous parallel connected SWCNTs [4]. It was suggested that both the resistivities of SWCNT bundle and MWCNT interconnects are smaller than that of Cu interconnects [5,6], and they have been identified as a promising candidate for future interconnects of integrated circuits [7].

Much effort has addressed the modeling of CNTs to accurately estimate the performance of CNTs interconnects. A single SWCNT was first equivalent to a distributed *RLC* transmission line based on the Lüttinger liquid theory [8], and then the transmission line (TL) model [9,10], the equivalent single-conductor TL model [11], and the multi-conductor TL model [12] were proposed for SWCNT bundle interconnects. On the other hand, the distributed equivalent circuit model [5] and single-conductor TL model [13] for MWCNT interconnects were proposed. Moreover, a compact physical model for MWCNTs was also proposed, and closed-form solutions to calculate their conduction channel numbers as well as conductivities were further derived [6,14]. In addition, the performance analysis for CNTs interconnects in propagation delay [15–18] and crosstalk [2,19–21] was widely reported.

Compared with traditional Cu interconnects, CNT interconnects are more susceptible to the inductance effect since their resistivity is smaller than that of Cu interconnects. Moreover, the inductance effect on interconnects will be more significant with increasing clock speeds, increasing wire lengths and decreasing signal rise time [22,23]. Hence, to accurately estimate the propagation delay of CNT interconnects, the *RLC* propagation delay model should be used rather than the *RC* propagation delay model [24]. There exists two closed-form propagation delay models for distributed *RLC* interconnects [23,25], but they will be suffered from large errors when the inductance effect is significant. In the third section of this paper, we will propose a new closed-form expression of 50%

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propagation delay for distributed *RLC* interconnects, to accurately estimate the propagation delay of CNT interconnects.

The focus of this paper is the performance analysis of propagation delay and repeater insertion for SWCNT bundle interconnects in the intermediate and global levels, to explore their feasibility in the application of future interconnects. Although this field has been researched in [26], the inductance effect of SWCNT bundle is neglected, and the *RC* propagation delay model and its corresponding repeater insertion model are used. Therefore, the obtained results are inaccurate. In addition, there is a wrong conclusion that the propagation delay of SWCNT bundle interconnects is linearly dependent on the wire length due to the very large effect of kinetic inductance, and repeater insertion is not capable of improving the propagation delay [11]. We find that the propagation delay of SWCNT bundle interconnects is also super-linearly dependent on the wire length similar to Cu interconnects, and repeater insertion can also effectively reduce the propagation delay. We also find that the optimum repeater number of SWCNT bundle interconnects to minimize the propagation delay is much smaller than that of Cu interconnects.

This paper is organized as follows. Section 2 extracts the equivalent circuit parameters (*RLC*) of Cu and SWCNT bundle interconnects. In Section 3, a new closed-form 50% propagation delay expression for distributed *RLC* interconnects is proposed, and then accurate closed-form solutions for the optimum repeater number and size to minimize the propagation delay are further derived. Using the proposed models in Section 3, the performance comparison between Cu and SWCNT bundle interconnects is carried out in Section 4. Finally, some conclusions are drawn in Section 5.

2. Electrical models of Cu and SWCNT bundle interconnects

For the purpose of comparison, we model Cu and SWCNT bundle interconnects in this section. To derive the equivalent circuit parameters (*RLC*) of interconnects, the interconnect structure as shown in Fig. 1 is used. In this figure, *W* and *H* are the width and height, respectively, *S* is the gap between adjacent interconnects and is assumed equal to be the wire width *W*, and *T* is the thickness of the interlevel dielectric.

2.1. Equivalent circuit parameters of Cu interconnects

The resistivity of Cu interconnects will become much larger than its bulk resistivity when the lateral dimensions are scaled down to the nanometer scale, which is attributed to the effects of grain-boundary and surface scattering, and can be expressed as [27,28]

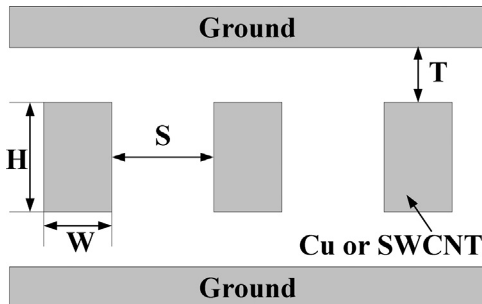

Fig. 1. Cross-sectional view of a typical interconnect structure.

$$\rho_{Cu} = \rho_0\left\{\left[1-\frac{3}{2}\alpha + 3\alpha^2-3\alpha^3 \ln\left(1+\frac{1}{\alpha}\right)\right]^{-1} + \frac{3}{8}C\frac{\lambda_0}{W}\cdot\frac{1+AR}{AR}(1-Q)\right\} \tag{1}$$

with

$$\alpha=\frac{\lambda_0}{d}\frac{R}{1-R} \tag{2}$$

where ρ_0=1.9μΩ·cm is the resistivity of bulk Cu, $C=1.2$ is a constant for rectangular cross-sections, λ_0=39nm is the electron mean free path for Cu at room temperature, *AR* is the aspect ratio (height over width), *d* is the average distance between grain boundaries, *Q* is the specular scattering coefficient at the surface, and *R* is the reflectivity coefficient at grain boundaries. In this paper, we assume $Q=0.5$, $R=0.5$, and $d=W$. So, the resistance of Cu interconnects is

$$r_{Cu}=\frac{\rho_{Cu}}{W\bullet H} \tag{3}$$

For the interconnect structure as shown in Fig. 1, the capacitance to ground c_g and the capacitance between adjacent interconnects c_m per unit length are given by [29]

$$c_g=\epsilon\left[\frac{W}{T}+2.04\left(\frac{S}{S+0.536T}\right)^{1.77}\bullet\left(\frac{H}{H+4.53T}\right)^{0.071}\right] \tag{4}$$

and

$$c_m=\epsilon\left[1.41\frac{H}{S}e^{-\frac{4S}{S+8.01T}} + 2.37\left(\frac{W}{W+0.308S}\right)^{0.257}\left(\frac{T}{T+8.96S}\right)^{0.757}e^{-\frac{2S}{S+6T}}\right] \tag{5}$$

where ε is the permittivity of the dielectric. The average capacitance per unit length for each Cu interconnect can be considered to be [30]

$$c_{Cu}=2\left(c_g+c_m\right). \tag{6}$$

The inductance per unit length of Cu interconnects can be calculated using [31]

$$l_{Cu}=\frac{\varepsilon_r}{c_0^2}\times\frac{1}{c_{Cu}} \tag{7}$$

where c_0 is the velocity of light in free space, and ε_r is the relative permittivity of the dielectric.

2.2. Equivalent circuit parameters of SWCNT bundle interconnects

For SWCNT bundle interconnects, the number of SWCNTs in the bundle is a critical factor to determine the equivalent circuit parameters and is given by [21]

$$n_{CNT}=\begin{cases} n_W n_H-\frac{n_H}{2}, \text{ if } n_H \text{ is even number} \\ n_W n_H-\frac{n_H-1}{2}, \text{ if } n_H \text{ is odd number} \end{cases} \tag{8}$$

with

$$n_W=\left\lfloor\frac{W-D}{D+d}\right\rfloor+1 \tag{9}$$

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