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A high linearity and high gain Folded Cascode LNA for narrowband receiver applications

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ABSTRACT

Folded Cascode (FC) Low Noise Amplifier (LNA) is preferred for low voltage and low power RF applications. A FC LNA with g_m-boosting technique is reported in the literature. Under low voltage operation, linearity of the LNAs is degraded due to transconductance and drain conductance nonlinearities. To improve the linearity of the LNAs, several techniques namely Harmonic Termination Network, Derivative Superposition, Modified Derivative Superposition (MDS) techniques are reported in the literature. In this paper to achieve high linearity for the g_m-boosting FC LNA, MDS technique is incorporated at the Common Source (CS) stage and is proposed. In order to evaluate the efficacy of this approach, the proposed LNA is designed and implemented in UMC 0.18 μm MMRF CMOS process for 2.44 GHz. From the simulation results, it is found that the proposed LNA achieves a gain (S_{21}) of 14.6 dB, Noise Figure (NF) of 2.9 dB, Input matching (S_{11}) of −15 dB and third order Input Intercept Point (IIP_3) of +4.19 dBm. The power consumption of LNA is 3.8 mW for a supply voltage of 0.6 V. The proposed LNA has a higher Figure of Merit (FoM) than that of other Cascode LNAs reported in the literature.

1. Introduction

CMOS technology scaling paves way for high degree on chip system integration with reduced power consumption. To realize key building blocks in RF and analog circuits, such as LNA and the power amplifier with low supply voltage is difficult, as these blocks have stringent performance criteria. Hence, it is difficult to achieve a high gain and high linearity for the LNAs in deep submicron process [1]. For low-voltage operations, Folded Cascode LNA is preferred over other LNA topologies. In FC LNA, the dominant source of nonlinearity is the transconductance nonlinearity at the common-source (CS) stage. To overcome this limitation, several techniques have been reported in the literature. An auxiliary path can be used for canceling the nonlinearity by adding the currents in the main and the auxiliary paths at the output node as reported in [2]. But this increases the power dissipation as an additional identical path is required. A more effective technique for narrowband applications proposed in [3], achieves high linearity by blocking nonlinear signals at a particular node by using harmonic termination network. In [4], optimum biasing is used to improve linearity. In this technique, the transistor is biased at the zero crossing of the third order nonlinearity component of the transconductance (g_{m3}). This reduces the third-order nonlinearity. But, it is sensitive to bias variation. Moreover, the second order nonlinearity transconductance component (g_{m2}) is large at this point, which may contribute to third order intermodulation component (IM3) due to source degeneration feedback. Externally generated second order intermodulation component (IM2) is added in [5] for cancellation of the nonlinearity at the output. But, due to IM2 generator there is significant noise contribution for single ended LNA. In [6] Derivative Superposition (DS) method is proposed for improvement of linearity in amplifiers. In DS method, the third order non-linear components of two transistors are strategically added by biasing the transistors in different regions of operations. This also reduces the sensitivity due to bias variations. In [7] multi-gated transistors (MGTR) technique or Derivative Superposition (DS) method is used for FC LNA without source degeneration for improvement in linearity. In source degenerated FC LNA [8], feedback of second-order non-linear component due to degeneration inductance contributes to third order non-linearity. Modified Derivative Superposition (MDS) technique is proposed in [9] for source degenerated LNAs to achieve high linearity. In this paper, to improve the linearity of the source degenerated g_m-boosted FC LNA [8], MDS technique is adapted at the Common Source (CS) stage, thereby a high gain and high linearity can be achieved for the LNA.

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The organization of the paper is as follows. Section 2 describes g_m-boosting FC LNA topology. Section III discusses the MDS technique for linearity improvement in low noise amplifiers. Section 4 gives the design details of the proposed LNA. Simulation results of the proposed LNA are given in Section 5 and conclusion is given in Section 6.

2. g_m-boosting Folded Cascode LNA

Cascode topology is widely used for LNA due to its advantages such as better gain, isolation, stability and impedance matching. Source degeneration inductor realizes resistive impedance without physical resistance. But due to stacking of transistors, there is a limitation of voltage headroom. To overcome this limitation, folded cascode topology [8] is preferred over cascode LNA. Fig. 1, gives the circuit diagram of the Folded Cascode LNA with source degeneration. M_1 and M_2 represent the Common Source (CS) and Common Gate (CG) stages respectively. Ls is the source degeneration inductance which is used for impedance matching at the input. Lo and Co are used for output matching. The LC tank circuit is realized using Lt, Ct and interstage parasitic capacitances associated at the cascode node. It resonates at the frequencies of interest and it also provides bias current for M_1 and M_2. The operating voltage of the folded cascode topology can be reduced by one overdrive voltage since there is no stacking of transistors. This leads to reduction of DC power consumption.

Higher gain in LNA reduces the noise figure constraints for the subsequent blocks in a wireless receiver. The effective gain of the FC LNA can be boosted by inserting an inverting amplifier between gate and source of CG stage [8] as shown in Fig. 2a. This is referred to as g_m-boosting technique. The small signal equivalent circuit is shown in Fig. 2b. This makes the effective transconductance of the CG stage to be $(1+A).g_{m2}$, where g_{m2} is transconductance of CG stage and A is the gain of the inverting amplifier connected between gate and source of CG stage.

The output voltage of the CG stage is given by

$$v_{out}=-(g_m v_{gs})R_L \tag{1}$$

where

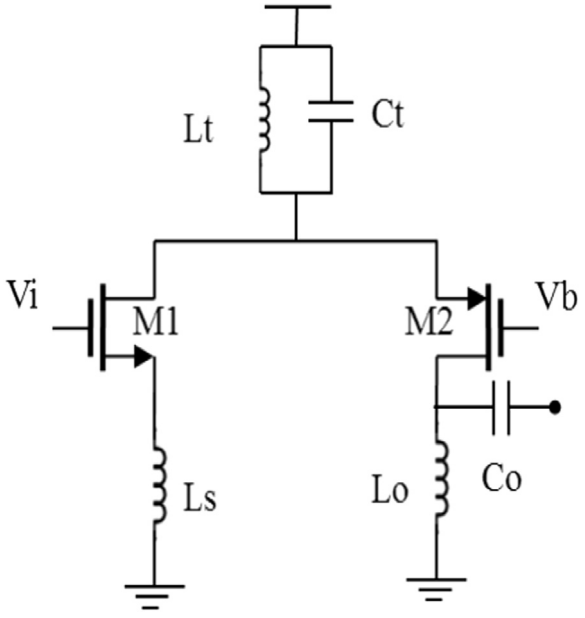

Fig. 1. Folded Cascode LNA.

$$v_{gs}=-(A+1)v_{in} \tag{2}$$

Using (1), the voltage gain is given by

$$A_v = \frac{v_{out}}{v_{in}} = g_m R_L(A+1) \tag{3}$$

3. Modified Derivative Superposition (MDS) technique

As the technology scales down, the short channel effects dominate [11], and the drain current $I_D$of MOS device is given by

$$I_D = \frac{1}{2}\frac{W}{L}\mu_o C_{ox}\frac{(V_G - V_T)^2}{1+\theta(V_G - V_T)} \tag{4}$$

where μ_0 is low field mobility and θ is fitting parameter.

The drain current i_d of the MOS device is given by

$$i_d = g_{m1}v_{gs} + g_{m2}{v_{gs}}^2 + g_{m3}{v_{gs}}^3 \tag{5}$$

In (5), g_{m1} is the main transconductance of the MOSFET, g_{m2} is the second order non-linear coefficient and g_{m3} is the third order non-linear coefficient. These coefficients are given by

$$g_{m1} = \frac{\partial i_d}{\partial v_{gs}},\ g_{m2} = \frac{1}{2}\frac{\partial^2 i_d}{\partial {v_{gs}}^2},\ g_{m3} = \frac{1}{6}\frac{\partial^3 i_d}{\partial {v_{gs}}^3} \tag{6}$$

From (4) and (5), it is clear that the MOS device exhibits non-linear behavior.

The IIP_3 of the non-linear device is given by [11]

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{7}$$

From (7), it may be noted that, to achieve higher IIP_3, g_{m3} has to be minimized.

In [8], the source degenerated inductor Ls is used for matching the input impedance. But the feedback due to Ls makes the second order harmonics ($\pm\omega_1, \pm\omega_2, \pm\omega_1 \pm\omega_2$) due to the nonlinearity of the amplifier to mix with the fundamental components. This results in IM3 components ($2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$) that leads to reduce the IIP_3. To improve IIP_3 of Cascode LNAs, MGTR (also referred to as DS method) is proposed in [6,7,15]. In DS, the IIP_3 is improved by reducing the effect of transconductance nonlinearity at the CS Stage. It does not reduce the IM3 components introduced by the source degenerated inductor Ls. Hence, DS method is not effective in reducing the IM3. To reduce IM3, MDS technique is proposed in [5]. Fig. 3 shows the realization of MDS technique proposed for the CS stage of a Source Degenerated LNA [9]. The MOS device in the CS stage and the degenerating inductors are split into two (M_1 and M_2) and (L_1 and L_2) respectively. The DC characteristics of the transistor (shown in Figs. 4 and 5) can be divided into three regions: strong inversion (SI), moderate inversion (MI) and weak inversion (WI). In weak inversion region, the induced gate noise of the transistor increases the noise figure since it is inversely proportional to the drain current. Hence, M_1 and M_2 are biased in the moderate inversion and strong inversion respectively. In MDS technique, the contribution of second order non-linearity to IM3 components is canceled by proper selection of L_1 and L_2. By proper selection of the sizes and bias conditions of the transistors, the third order non-linearity can be canceled. The second order non-linear coefficient (g_{m2}) and third order non-linear coefficient (g_{m3}) are obtained as a function of gate to source voltage (V_{GS}) through simulation and are shown in Figs. 6 and 7. The second and third order nonlinear component of the transistors M_1 and M_2 are represented as (g_{m21} and g_{m22}) and (g_{m31} and g_{m32})