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Design of a practical fault-tolerant adder in QCA

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ABSTRACT

Quantum-dot cellular automata (QCA) has emerged as an attractive alternative to CMOS technology in nanoscale era. QCA-based circuits often suffer from various types of manufacturing defects and variations, and therefore, are unreliable and error-prone. Hence, developing fault-tolerant circuits are essential for their reliable realizations. Design of QCA adders have been studied extensively due to its frequent use in the construction of several computing subsystems including arithmetic and logical units (ALUs). Most of the existing QCA adder designs have ignored fault-tolerance against various defects relevant to QCA. Although, a few of them have studied the behavior of their design in presence of some possible defects, poor defect coverage and/or low fault-tolerance make them unsuitable for practical realizations. In this paper, we propose a QCA adder that shows significant fault-tolerance against all types of cell misplacement defects such as cell omission, cell displacement, cell misalignment and extra/additional cell deposition. In order to judge practical realizability of the proposed design, we have compared it with the existing adders in terms of both fault-tolerance and other commonly accepted design metrics such as area, delay, complexity, cost of fabrication, and irreversible power dissipation. The detailed comparative study reveals that the proposed adder not only offers significantly high degree of fault-tolerance but also performs fairly well as compared to the existing adders with respect to other design metrics too, thereby ensures practical realizability of the proposed adder.

1. Introduction

In the last six decades, CMOS based semiconductor industry has witnessed a tremendous growth in device integration. This is achieved by continuous downscaling of device feature size confirming Moore's prediction [1]. However, it is expected to reach its physical limit in the near future [2]. In order to cope up with this, researchers across the globe are making sincere efforts to explore alternative nanotechnologies. Quantum-dot cellular automata (QCA) [3] has emerged as one such prognosticating alternative to CMOS technology. Extremely low power consumption and dissipation [3], high device packing density, high speed (in order of THz), inherent pipelining [4] are some of its prominent features which have drawn huge attention in recent past. In QCA, logic states are encoded as the orientations of two electrons (often called as polarization states) which are present in diagonally opposite charge containers (referred to as quantum dots) on the four corners of a square-shaped element (referred to as cell). In QCA, information flows through the cells not by actual flow of current, as in conventional CMOS based designs, but by Coulombic interactions between electrons present in neighboring cells resulting in very low power dissipation [3].

For the last two decades, a major part of the research on QCA has focused on the design and simulation of various digital modules including basic logic gates [4], adders [5–9], multipliers [8,10], dividers [11,12], linear feedback shift registers (LFSRs) [13,14], parity generators [15], decoders [16,17].

As in other nanotechnologies, the manufacturing process of QCA is yet to mature for commercial production and hence, suffers from a high defect rate [18–20]. Several attempts to characterize QCA manufacturing defects have been made in recent past [21,22]. Manufacturing defects in QCA may be introduced in both the chemical synthesis phase as well as the deposition phase [21]. However, *cell misplacement* defects introduced in the deposition phase have been found to be more frequent [21]. Several types of cell misplacement defects viz. *cell omission*, *cell displacement*, *cell misalignment*, and *extra-cell deposition* have been reported in the literature so far [21,22]. These defects have cataclysmic consequences on the performance of QCA logical devices [22]. Hence, design of fault-tolerant QCA circuits are essential for their reliable realization. A few work on fault-tolerant design of QCA circuits [23–26] have been proposed in recent past.

Design of adders have been studied extensively due to its frequent use in the construction of several computing subsystems including arithmetic and logical units (ALUs). Several designs for QCA adders [5–9,27,28] have appeared in the literature so far. The design metrics that have been considered as the optimization goal

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Table 1
Comparison of fault-tolerance of the existing adders against various cell misplacement defects.

Defect type	Fault-tolerance† (%)					
	Sen adder [27]		Roohi adder [28]		Farazkish adder [24]	
	Sum	Carry	Sum	Carry	Sum	Carry
Single-cell omission	11.54	76.92	22.22	72.22	48.59	95.94
Double-cell omission	NA	NA	NA	NA	NA	NA
Extra cell	92.39	100	57.69	67.31	NA	NA
Cell displacement/ misalignment	5.88	5.88	25.64	25.64	55.55	55.55

† The details are presented in Section 5.

in these designs are the number of cells, area, delay, the number of QCA logic gates, and the number and type of crossovers [29]. Unfortunately, a very few of the existing QCA adder designs [24] have considered fault-tolerance as a design optimization goal. Moreover, the designs that claimed to be fault-tolerant [24,27,28] fail to show significant defect coverage and/or fault-tolerance, thereby making them unsuitable for practical realizations. Table 1 shows a summary of various defects considered and the fault-tolerance achieved by these adder designs.

In this paper, we propose a QCA adder that shows significant fault-tolerance (more than 90%) for various types of cell misplacement defects such as single-cell omission, extra-cell deposition, cell displacement and misalignment. Simulation results are presented based on semiconductor implementation of QCA with an intermediate dot size of about 5 nm (which is different from magnetic QCA or molecular QCA in which dot sizes are approximately 100 nm and 2–5 nm respectively [25]). Additionally, the proposed adder performs fairly well against multiple cell omissions also. Note that a practical design must not compromise in one design metric (beyond an acceptable level) for the sake of optimizing the other. In order to judge the practical realizability of our design, we have compared it with the existing adders in terms of both fault-tolerance and other commonly accepted design metrics such as area, delay, the number of QCA logic gates, and the number and type of crossovers [6,8,29]. The comparative study reveals that the proposed design not only offers significantly high degree of fault-tolerance but outperforms many existing adders with respect to other design metrics too.

The remainder of the paper is organized as follows. Section 2 elucidates the preliminary concepts about QCA. Section 3 reviews the existing adder designs. Design and simulation of the proposed fault-tolerant adder is presented in Section 4. Section 5 presents the degree of fault-tolerance achieved by the proposed adder as compared to the existing adders. Comparative study with the existing adders in terms of other commonly accepted design metrics is presented in Section 6. Finally, conclusions are drawn in Section 7.

2. Basics of QCA

Quantum-dot cellular automata (QCA) has emerged as a novel paradigm for computing at the nanoscale. The basic principle of operation is based on quantum–mechanical effects and the quantization of charge [3]. The elementary building block of QCA is a square-shaped charge-containing structure known as *QCA cell*. A QCA cell consists of four potential wells (dots) located at the four corners of the cell and two free electrons which can tunnel quantum mechanically from one dot to another. Due to Coulombic repulsion, the two electrons within a cell always tend to occupy

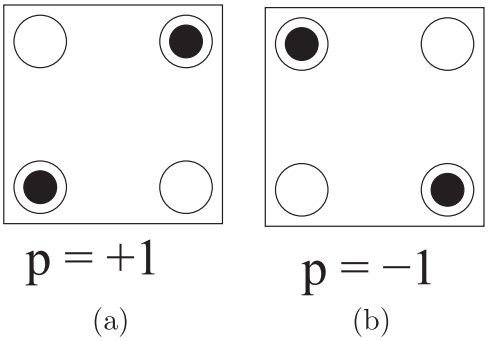

Fig. 1. QCA cell with (a) $p=+1$ and (b) $p=-1$.

antipodal sites resulting two energetically equivalent minimal arrangements. These two arrangements, often denoted as *cell polarization (p)*, are used to encode binary information. Fig. 1(a) and (b) show QCA cells with $p=+1$ and $p=-1$ respectively. These two polarization states are used to represent logic 1 and logic 0 respectively.

Unlike conventional CMOS technology, information flow in QCA is achieved by Coulombic interactions between the electrons present in neighboring cells and is independent of actual flow of current. The simplest arrangement of QCA cells is given by placing them one after another in series forming a QCA wire. If the polarization of the leftmost cell is forced to assume a particular state by applying external electric field, the rest of the cells would immediately synchronize to the same polarization due to Coulombic interactions between them. Fig. 2 shows one such arrangement called as *binary wire*. There is another type of QCA wire (called as *inverter chain*) that is used to transfer data from one place to another. In an inverter chain, all the cells are 45° rotated from the normal QCA cells. As shown in Fig. 3, each cell of the chain inverts the logic state of its preceding cell. Hence, the final output can be same or the inverted value of the input depending on whether the number of cells between input and output is odd or even.

Majority voter (MV) and *inverter gate* are considered as the two most fundamental building blocks of QCA [4]. Typical designs of a three input majority gate and an inverter are shown in Fig. 4 (a) and (b), respectively. AND and OR gates can be constructed using the majority gate easily by forcing one of the inputs of the majority gate to logic 0 and logic 1, respectively [4].

A number of other implementations of majority voter and inverter gates have been reported in the literature [26,30,31]. Fig. 5 (a) and (b) show some other possible implementations of QCA inverter.

Alike CMOS, QCA circuits also require a clock to function properly. The QCA clocking scheme serves two purposes: powering the automaton, and controlling (synchronizing) the data transfer. It facilitates the movement of electrons within a cell and allow them to change their configuration in a predefined manner by changing the tunnelling barrier between quantum dots [32]. Typically, a four-phase clocking scheme [32] is used (Fig. 6).

There are four clock zones with a 90° phase shift from one clocking zone to the next. Each clock zone uses four phases namely *hold*, *release*, *relax*, and *switch*, respectively. The tunnelling barrier of the quantum dots is kept high at the hold phase, which keeps the electrons in a fixed polarization state. During the release phase, the electrons are allowed to move slowly by decreasing the

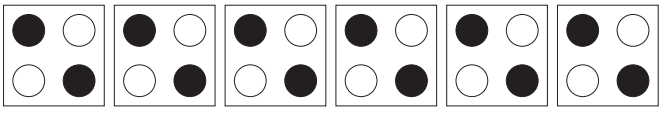

Fig. 2. QCA binary wire.