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Modeling and analysis of single-event transient sensitivity of a 65 nm clock tree

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ABSTRACT

The soft error rate (SER) due to heavy-ion irradiation of a clock tree is investigated in this paper. A method for clock tree SER prediction is developed, which employs a dedicated soft error analysis tool to characterize the single-event transient (SET) sensitivities of clock inverters and other commercial tools to calculate the SER through fault-injection simulations. A test circuit including a flip-flop chain and clock tree in a 65 nm CMOS technology is developed through the automatic ASIC design flow. This circuit is analyzed with the developed method to calculate its clock tree SER. In addition, this circuit is implemented in a 65 nm test chip and irradiated by heavy ions to measure its SER resulting from the SETs in the clock tree. The experimental and calculation results of this case study present good correlation, which verifies the effectiveness of the developed method.

1. Introduction

Single-event upsets (SEUs) in storage elements [1] and single-event transients (SETs) in combinational logics [2] are the two main modes of soft errors caused by radiation. Previous studies have pointed out that the soft error rate (SER) ratios contributed by SEUs and SETs depend on clock frequency [3, 4]. At the high frequency end, SETs can be the dominant factor determining the overall SER, due to the increased probabilities for them to be captured at clock edges [3]. Because higher performance is one of the major factors driving the technology evolution, the SET issue is expected to be more severe in advanced technologies [2]. The SETs in clock networks, as special cases of combinational SETs [5], can also impose threats on digital circuits' reliabilities. The severity of clock SETs partially comes from the global nature of clock signals. Different from the data path SETs that are commonly localized, an SET at a clock node can propagate through the following branches and incorrectly trigger a large number of flip-flops [6]. The lack of logical masking can be another reason easing the clock SET propagations, since a clock network can be typically constructed by using inverters and buffers only [6].

Studies have been performed to investigate the SET sensitivities of clock networks. In [7], heavy ion experiments on a 90 nm radiation hardened by design (RHBD) processor identify the clock SETs induced errors in flip-flops. Hansen et al. distinguished the heavy ion SERs of combinational, sequential, and clock tree parts of 90 nm test circuits and found that the saturated SER of the studied clock tree at the high linear energy transfer (LET) end was similar to that of the unhardened flip-flop [8]. Heavy ion test results of a 28 nm clock mesh illustrate that, although the mesh itself is well hardened, burst errors in flip-flops can still occur due to the propagations of SETs at the pre-mesh drivers [9]. All of these studies provide evidences showing that clock networks can be important sources of soft errors. In [10], the fault modes of clock SETs are differentiated as race and jitter. The former one refers to individual SET pulses that can trigger flip-flops, while the latter is the random movement of clock edges as results of the merging of SETs and clock waveform [10]. Longer data path delays can help avoid the effect of clock races, since they can maintain the old data at the flip-flops' inputs longer and thus clock SETs may only trigger flip-flops to sample the same data again, which will not lead to data corruption [10]. On the other hand, data paths with longer delays can be more vulnerable to clock jitters, because the shortened clock periods can introduce setup time violations for these paths [10].

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Efforts have been made on the SER modeling and prediction for clock networks. The work in [11] developed an EXT-CLK tool to extract the clock tree structure from a given circuit. The extraction result is a SPICE netlist of the clock tree. Fault-injection simulations then are performed on the netlist to evaluate its radiation sensitivity. The nature of SPICE simulations allows accurate modeling of the electrical masking effect. However, there are still two issues that need further consideration for this method. First, the double exponential current model is used for fault-injections. Because this model does not take the interactions between circuit responses and single-event currents into account, it may result in low accuracy in advanced technologies [12]. Second, this method may have low time efficiency, since performing exhaustive analysis of all clock nodes of a large scale design in a SPICE environment could be time consuming.

Another tool called SEUTool was developed to predict the SERs of synchronous digital circuits [13, 14]. It was first applied on a 250 nm 4-bit bit-slice processor [13]. Then this tool's effectiveness was experimentally evaluated on a 150 nm silicon-on-insulator (SOI) digital signal processor, and good analysis accuracy and performance were shown [14]. Furthermore, this tool can perform analysis for both sequential SEUs and combinational SETs [14]. Therefore, in principle it should also be capable of handling clock SETs analysis. Some considerations are needed when applying this tool on nanoscale circuits. First, it also uses the double exponential current model for the radiation characterizations of logic gates, which may introduce inaccuracy, as mentioned above. Second, this tool estimates the sensitive areas of logic gates mainly based on the transistor areas. Some secondary effects, e.g., bipolar amplifying, induced sensitivity increase is simply modeled by multiplying the transistor areas by a fixed number (6 for the 150 nm SOI in [14]). It seems not very clear if this concept of simplification can be transferred directly to a smaller technology. It is also noted that the SEUTool takes the amount of collected charge as an independent variable, and this amount needs to be converted into an LET value later. This conversion may not be very straightforward and can be another source of inaccuracy [14]. As discussed in [14], all these issues above can be overcome through well calibrated TCAD simulations on single gates. In this way, various factors can be considered at the same time, and less “guesswork” and simplifications would be needed [14]. This actually emphasizes the criticality of accurate single-event characterizations of fundamental cells for the SER analysis of a system composed of those cells, which is also the idea of this work.

This paper aims to develop a method for the flexible and high efficiency prediction of clock tree SER. This method first utilizes a dedicated soft error analysis tool TFIT to perform SET characterizations of clock inverters in various conditions. The characterization results are organized as clock inverters' radiation response databases that can be reused later for any clock tree structures. Other electronic design automation (EDA) tools are used to extract required information from designs, generate SET injection stimuli, and perform fault-injection simulations to calculate the SERs of clock trees. Since the fault-injection simulations are completed in a Verilog environment, much higher time efficiency can be enabled. A test circuit in a 65 nm Complementary Metal-Oxide Semiconductor (CMOS) bulk technology is taken as an example to predict its clock tree SER through the developed method. This circuit is also implemented in a test chip in the same 65 nm technology and irradiated by heavy-ions to measure its clock tree SER. The predicted and experimental results show relatively accurate correlation, which verifies the effectiveness of the developed method.

The rest of this paper is organized as follows. Section 2 details the proposed clock tree SER prediction method. Section 3 describes the test circuit and illustrates its predicted and experimental clock tree SER results. Discussions on these results are given in Section 4. This paper is concluded in Section 5.

2. Framework

The proposed method consists of three steps: 1) SET characterizations of clock inverters, 2) parameter extraction of a given design, and 3) SER prediction through fault-injection simulations. All these steps are detailed as follows.

2.1. SET characterization

For a given clock inverter, its SET sensitivity depends on three factors: 1) the LETs of incident particles, 2) the capacitive load of its output node, and 3) the logic state (indicated by its output level). The first factor directly affects the amount of single-event charge deposited while the second one can modulate the nodal critical charge amount. It should be noted that the second factor also includes the parasitic capacitances of interconnection wires. The logic state of a clock inverter determines the location and area of the sensitive drain and which device (nMOS or pMOS) will provide restoring current during a single-event process. It is noted that the transistor sizes of a clock inverter also affect the radiation responses significantly because they can determine the restoring currents. As will be discussed later, the transistor size information is included in the SPICE netlist of the inverter under analysis. By using this netlist as an input of the SET characterization, the restoring currents of transistors can be modeled accurately.

Different from sequential SEUs, a clock inverter's SET sensitivity cannot be described by just one cross section value but instead by a cross section distribution as a function of pulse width range. In the proposed method, with a set of LET, capacitive load, and logic state, a 65 nm clock inverter's SET cross section distribution is characterized within ranges $(7.5 + (n\text{-}1) \times 20, 27.5 + (n\text{-}1) \times 20)$ ps, $n = 1$–22, and each range has a length of 20 ps, which is similar to the resolutions of some SET measurement circuits in 65 nm [15]. The SETs shorter than 7.5 ps are not considered. This is because the minimum inverter delay in this 65 nm is slightly longer than 7.5 ps. Therefore, a < 7.5 ps clock SET is short enough to be electrically filtered by the following inverters and cannot propagate in the clock tree.

In this paper, the clock inverter selected from the 65 nm standard cell library for study is CINVD0. The postfix “D0” in its name indicates that it is of the minimum driving strength within its logic function family. The TFIT, a cell-level SER simulation software from iROC Technologies [16, 17], is applied to perform the SET characterizations described above for CINVD0. The netlist with parasitics (in SPICE format) and layout file (in GDS format) of CINVD0 are read by the TFIT as inputs. The TFIT analysis requires a technology-specific radiation response model. This model is pre-characterized through technology computer aided design (TCAD) simulations to contain the single-event responses of transistors [17]. In this paper, a generic model for 65 nm bulk CMOS is used. It should be noted that, although the TFIT can provide desirable accuracy and efficiency, the developed method in this paper actually does not strictly rely on this tool. Other characterization techniques may also be embedded. For example, it is possible to use the physics-based engineering method studied in [18], which successfully predicted the heavy-ion cross sections of a 90 nm SRAM cell, to carry out the SET characterizations required in this paper. However, migrating a single-event analysis method from one technology to another may not be straightforward, because the method commonly can rely on certain technology related parameters and those parameters can be unknown for the target technology. Therefore, more efforts can be required to extract those parameters typically by means of TCAD simulations and experimental correlations. Given these, the TFIT (or other professional tools) may still be preferable, since it can provide users a unified analysis flow while the technology related information necessary for single-event analysis has already been packaged into the radiation response model. In a TFIT analysis, the tool calls a SPICE simulator to perform a set of circuit-level fault-injection simulations and then collects the results from them to calculate the cross section.

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