Asymmetric resistive switching behaviour in a Au/a-C:Co/Au planar structure

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A B S T R A C T

Using a simple fields induced mass motion method, Au/a-C:Co/Au planar structures with micro-gap Au electrodes were fabricated. Asymmetric current-voltage characteristics and resistive switching behaviours were observed in these cells. Reliable performance, with a reasonable ON/OFF ratio of > 4, stable endurance of > 200 cycles, and good retention of > 10^5 s, were achieved at the read voltage of -3.6 V. Space charge limited current (SCLC) theory with an asymmetric potential barrier caused by different densities of traps was proposed to explain the asymmetric resistive switching behaviour.

1. Introduction

Resistive random access memory (RRAM) has been proposed as a potential candidate for the future memory device due to its ultra-high operation speed, low energy consumption, long retention time and reducible size [1, 2]. Many types of materials have been verified to have resistive switching (RS) characteristics, such as binary transition metal oxides, complex perovskite oxides, organic materials, chalcogenides and others [3–5]. Such switching behaviours are also observed in carbon-based materials, including amorphous carbon (a-C), diamond-like carbon, carbon nanotubes and graphene oxide [6–8]. Among them, a-C shows considerable advantages as storage media materials, including low cost, well-developed manufacturing technique and satisfactory switching properties [9]. In our previous work, reliable and reproducible resistive switching phenomena have been studied in Cu/a-C/Al and Al/a-C:Co/FTO sandwiched structure devices, and the cobalt implanted a-C films exhibit good retention characteristics [10, 11].

Generally, RS effects are classified into unipolar and bipolar resistance switching behaviours (URS and BRS). Most researchers focus on the mechanisms of these two conventional RS behaviours. Currently, several groups have reported a new asymmetric resistive switching (ARS) behaviour in carbon-based materials. Zhao et al. realized both non-volatile and volatile RSs in Cu/a-C/Pt sandwich structure memory cells [12]. Moreover, the switching between rectified and non-rectified RS was observed to depend on the thickness of a-Si in the M/a-Si/p-Si structure according to S. Jo et al. [13]. They all attribute the RS behaviour to the asymmetric formation and rupture of conducting filaments between active and inert electrodes, while no sufficient explanation is considered for the ARS behaviour in the symmetric structure.

In this work, Au electrode pairs were used to form a symmetric Au/a-C:Co/Au planar structure cell to avoid the asymmetric effect due to different electrodes. Here, we put forward a practical method to build electrode pairs with nanometre-sized gaps (micro-gap) through a field-induced break-junction (FIBJ) technique [14]. ARS behaviour is observed in this symmetric Au/a-C:Co/Au planar structure cell. The asymmetric potential barrier caused by the different trap density in space charge limited current (SCLC) theory is regarded as an appropriate explanation to study the ARS behaviour in a symmetric structure. An intensive study of ARS behaviour will enrich investigations on the RS effect and lead to a better understanding of the RS mechanism. In addition to the mechanism research, the ARS effect exhibits an applied importance for its rectification characteristics. The cross-talk between the adjacent devices in the cross-bar circuits can be eliminated by the ARS behaviour [15].

2. Experimental

The preparation process flow of the symmetric Au/a-C:Co/Au planar structure cell is shown in Fig. 1. Amorphous carbon-cobalt
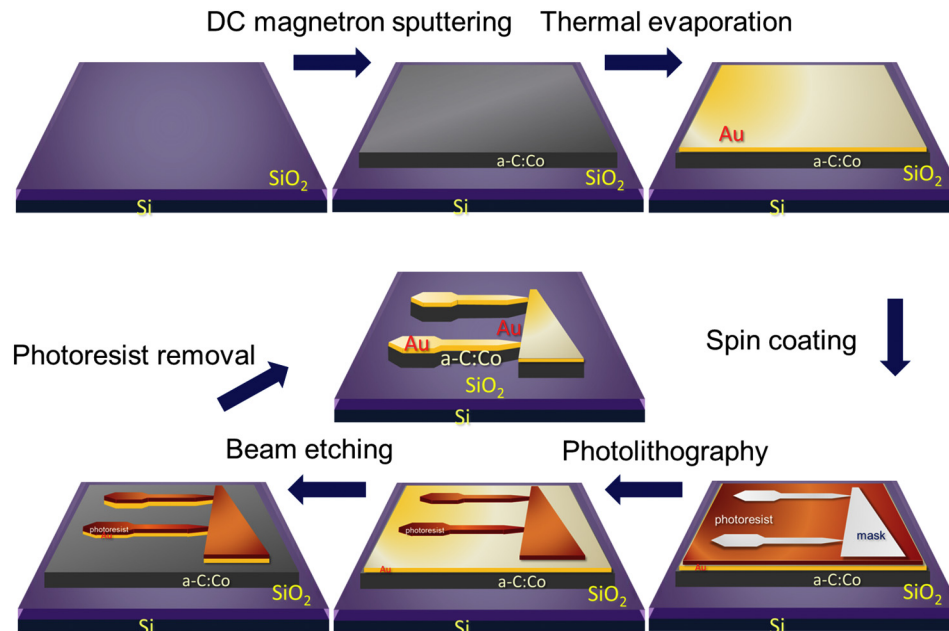

Fig. 1. (Colour online) The schematic of sample preparation flow.

composite (*a*-C:Co) films with a thickness of 300 nm were deposited on SiO$_2$(300 nm)/Si substrates by DC magnetron sputtering. To simulate the cobalt particle influence in a next generation low resistance connect line process, a commercial composite target (C: 96 at.%, Co: 4 at.%) was used to prepare the dielectric layer. During room temperature deposition, the argon pressure was maintained at 0.65 Pa, while the sputtering power kept at 100 W. Then, a gold layer (~60 nm) was thermally evaporated on the as-grown *a*-C:Co films. Au electrodes with micro-constriction were fabricated by the standard photolithography technique and followed by argon ion beam etching process. The etching time was adjusted to remove both Au and *a*-C:Co layers within the exposed areas. Finally, the remaining photoresist was removed by a chemical solution process.

Raman spectroscopy (JY, HR800UV) using wavelength of 514.5 nm was introduced to investigate the amorphous carbon films composite features. The surface morphologies of the Au electrodes and micro-gaps were observed by scanning electron microscopy (SEM, JSM-6330F). Elemental mapping was performed using an energy dispersive X-ray spectrometer (EDS, Bruker XFlash6160) attached to the SEM instrument. The I-V characteristics of the Au/*a*-C:Co/Au RRAM cells were measured using the Keithley 2400 semiconductor characterization system.

3. Results and discussion

Fig. 2a presents the Raman spectrum of as-deposited *a*-C:Co thin films. By fitting the measured spectra and decomposing it into individual Gaussian components, a relatively sharper G peak (centred at 1567.4 cm^{-1}) and a broad shoulder D peak (centred at 1354.4 cm^{-1}) were achieved. The coexistence of broad D and G peaks, corresponding to disordered microcrystalline graphite and sp^2 graphitic carbon respectively, demonstrates the amorphous feature of the as-deposited carbon films [16]. The third S peak, centred at 1456.7 cm^{-1}, was attributed to the C=C bonds in the *a*-C:Co films [17]. EDS elemental mapping illuminates the uniform distribution of Co in the *a*-C:Co film after electromigration (see Fig. 2b, c, d). The concentration of Co was found to be 5.27 at.%, which is slightly higher than that in the composite target. According to the EDS line scan in Fig. 2e, a residual thin layer of carbon is present between the electrode pairs. Therefore, the structure is considered a Au/thick *a*-C:Co layer under the electrode/thin

a-C:Co in the gap/thick *a*-C:Co layer/Au. A thick *a*-C:Co layer is introduced to modulate the resistance to obtain the appropriate operating current of ~10 μA [13].

Fig. 3a presents the plan view SEM image of as fabricated RRAM cell, before the FIBJ process. It exhibits a tiny connection between two electrodes. Hereafter, the FIBJ technique was conducted at room temperature, to realize forming process. Schematic of the FIBJ test structures is shown in Fig. 3b. A linearly increasing voltage *V* was ramped across the Au layer in steps of 200 mV. The monitored current-voltage (I-V) characteristics through the Au layer during fields induced mass motion are shown in Fig. 3c. Reaching to threshold voltage (~7 V), a sharp decrease current was observed, indicating that a micro-gap between two newly formed Au electrodes was created. Fig. 3d shows the scanning electron microscopy (SEM) image of a typically freshly fabricated micro-gap. Before the I-V measurement, micro-gaps in the devices exhibited ~100 nm separation with high tunnel resistance above 1.8×10^6 Ω. The positions of micro-gaps were controlled by the constriction structure. It is worth mentioning that a micro-gap of the underlying *a*-C:Co layer was also formed during this fields induced mass motion process, as confirmed by the EDS element mapping results (see Fig. 2), differing from previous reports [18].

After the electromigration process, I-V characteristics of the Au/*a*-C:Co/Au RRAM cells were measured in direct current sweeping mode (see Fig. 4). The ramp rate of the voltage sweep was set as 0.12 V/s. After each voltage step, the current was read and recorded. A compliance current (I_{CC}) of 1×10^{-5} A was applied to avoid the breakdown of the RRAM devices. The device with the identical material (Au) to the anode and cathode shows an obvious asymmetric RS performance with the voltage sweeping in the range of −6 V up to 6 V. For positive voltage scans (path 1 and path 2), no resistive switching behaviour was observed. With the applied bias decreasing from 0 V to −6 V (path 3), the device turned into the high resistance state (HRS), and a set-like change occurred at approximately −4 V (V_{set}). Then, the current flowing during the set transition was externally limited to I_{CC}, and the device was in the low resistance state (LRS). In the following voltage sweep measurements from −6 V to 0 V (path 4), the LRS could not be retained and showed a reset-like change at approximately −1 V (with an obvious slope change).

The endurance and retention time are known to be two important criteria in memory applications [19]. During the endurance tests, the