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Source engineering on ruggedness and RF performance of n-channel RFLDMOS

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ABSTRACT

The state-of-art n-channel RFLDMOS (Radio Frequency Lateral Double-diffusion Metal Oxide Semiconductor) FETs with different source engineering have been fabricated using 0.18 μm BCD (Bipolar/COMS/DMOS) process. The ruggedness and RF performance of RFLDMOS have been studied with TLP (Transmission Line Pulse) test, VSWR (Voltage Stop Wave Ratio) test, and source/load-pull test. It was found that PBL (P+ buried layer) source engineering could improve its ruggedness remarkably. The mechanism of this improvement has been studied by introducing equivalent parasitic circuit. The dominant factor is the resistor R_B which delays turn-on characteristic of parasitic NPN in equivalent circuit. And the computational model of R_B is proposed. Furthermore, the optimal performance of RFLDMOS has also been discussed.

1. Introduction

While p-channel LDMOS is competent for switching applications [8], n-channel LDMOS is usually used in RF power applications. RFLDMOS FETs are widely used in transceivers, broadcasts, radar, base stations as power device, for its cost, different operation voltages, and wide frequency band in recent decades [15].

Nowadays, obtaining good RF performance and outstanding reliability at the same time becomes the most important and challenging task for RFLDMOS design. These factors, such as frequency bandwidth, gain, output power, efficiency, noise, non-linearity, and so on, are selectively used to assess the performance of different RF applications. Reliability issues of MOSFETs, such as HCI (Hot Carrier Injection) and NBTI (Negative Bias Temperature Instability), had been analyzed and discussed in [16–18]. And ruggedness which indicates the ability of a device withstands unusual electrical condition without degradation [13] is also momentous reliability factor of RFLDMOS [5–7, 10, 13].

In order to study the ruggedness of DUTs (Device Under Test), many test methods had been introduced, such as TLP test on wafer and packaged level [1], ESD (Electro-Static Discharge) sensitivity test and VSWR susceptibility test for RF/microwave devices on package level, and so on. ESD sensitivity test is a kind of voltage zapping test for packaged DUT, after each zap the system will estimate whether the DUT fail or not by verifying its characteristic curve, and finally get the ESD sensitive voltage which is classified in different levels. On the other hand, TLP system can extract every current and voltage during each zap, and these values can be plotted as I-V curve. TLP test standard [2] and industrial TLP apparatus are available to researchers all around the world. Though TLP I-V curves had been studied a lot in ESD structures [3, 4] and LDMOS [5–8], different curve forms among them had seldom been analyzed deeply in terms of different structure engineering.

Structure engineering is a general method of optimizing the characteristics of LDMOS. When LDMOS used in ESD protect units, source-side and drain-side SCR (Silicon Controlled Rectifier) structures can bring it into latch-up state and conduct large current without destruction [19]. In RFLDMOS, structure engineering has been done carefully because unexpected parasitic capacitors degrade key parameters, such as transconductance, cut-off frequency, and so on [20]. So, PBL source-side engineering, which has small effect on RF performance, is applied in our RFLDMOS.

The aim of this paper is interpreting ESD failure mechanism of RFLDMOS FETs with and without source engineering during ESD event and estimating their overall performance. In this paper, the state-of-art RFLDMOS FETs with and without source engineering and TLP test principle will be introduced in section II. Then, equivalent circuit and key parameters will be modeled and calculated in section III. Next, two kinds of test curves will be analyzed with equivalent circuit models and key parameter models, also semiconductor physics theories will be adopted to interpret these phenomena in section IV. In section V, source/load-pull test and VSWR susceptibility test are used to study the

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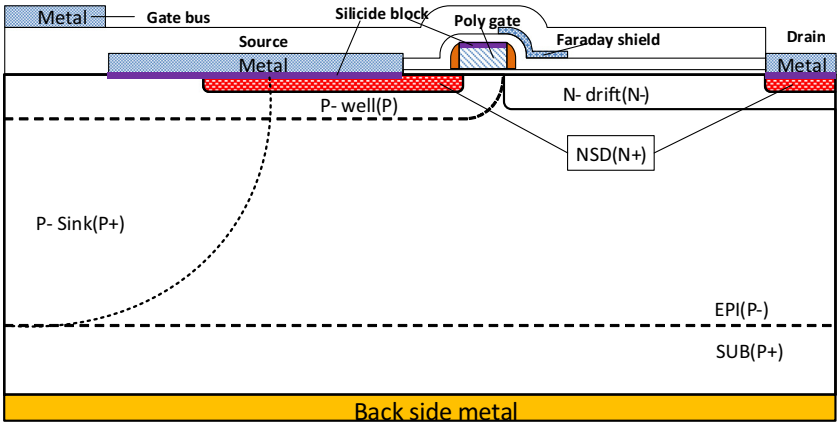
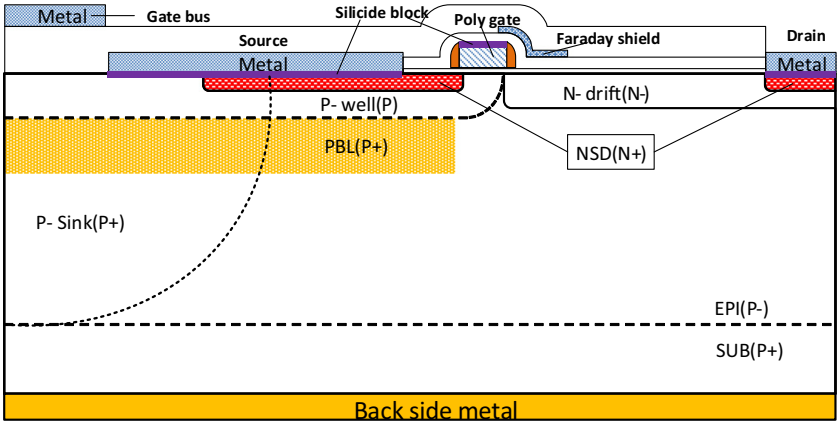


(a)



(b)

Fig. 1. The cross-section of RF LDMOS, (a) Type A: without PBL, (b) Type B: with PBL.

RF performance of DUTs.

2. RFLDMOS structure and TLP system for ruggedness test

According to RESURF (REduced SURface Field) technique [7], LDMOS has been designed with a low doping N-type area in the drain side to withstand high breakdown voltage. In Fig. 1, a half of one single finger's cross-sections, with and without source engineering, has been illustrated. Unlike using LOCOS (LOCal Oxidation Silicon) and extending gate to adjust surface field, Faraday shield, which is connected to source metal with metal lines and through the via, has the same function. Moreover, Faraday shield can minimize the feedback capacitance C_{dg} to improve RF and microwave characteristics [8]. In addition, silicide blocks have been fabricated on the surface of poly gate and source/drain metal contact to minimize contact resistance. P-sink connects source and substrate to decrease source parasitic inductance. When DUTs are used in power application, multi-finger structure is adopted to output large power and dissipates large current in it at the same time. In Fig. 1 (b), high dosage P-type ions have been implanted in source side with over 300KeV energy to form the P+ buried layer, where the gate self-align technique provides a specific position for it. These devices were processed in 0.18 μm BCD technology, and 0.6 μm gate length was chosen to obtain sufficient channel width, which is decided by the double diffusion conditions.

TLP test (Pulse width is about 100 ns) is used to model Human Body Model (HBM) while VF-TLP (Very Fast TLP, which has much shorter pulse width, such as several ns) is used to model Machine Model (MM) [9]. These two tests both can be conducted in one TLP test system, which is consisted of transmission line system, high speed oscilloscope, mechanical test bench with calibrated cables, and computer control system. Since the transmission line can hold high stable voltage without parasitic elements, high voltage and short pulse signals are obtained and applied in the terminals of devices or circuits. These signals are used to mimic ESD stress which is confronted by devices and circuits confront in real world. After each pulse zap, 1 V DC voltage will be applied to measure the leakage current of the terminals. This current is used to judge whether the device or circuit degrade or not. Because of short pulse width, high speed oscilloscope is needed to collect the current and voltage during each zap. Computer control system not only controls test process, but also records computed data into data files. The most important thing is that each point in TLP curve is the collection of former points. In another way, the former points happened if we want this point happen [12]. So, accumulation effect should be paid attention.

Three general ruggedness diagrams for different devices are illustrated in Fig. 2. Figure (a) shows TLP I-V curve of MOSFET [3, 4, 14] and HVNSCR [19], $V_{t2} > V_{t1}$ or higher I_{t2} means better ruggedness. Figure (b) is found in [7, 8, 11, 19], it exits in high-voltage transistors especially former LDMOS. After structure engineering, different I-V curve for more rugged device are show in (c) [5, 6, 8]. In this work, figure (b) and (c) will be discussed in the coming parts.