Microelectronics Reliability 87 (2018) 213–221

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

# Thermal annealing studies in epitaxial 4H-SiC Schottky barrier diodes over wide temperature range

P. Vigneshwara Raja[a], N.V.L. Narasimha Murty[b,*]

[a] Micro-fabrication and Characterization Lab, School of Electrical Sciences, IIT Bhubaneswar, Odisha 752050, India
[b] Electrical Engineering, IIT Tirupati, Tirupati, Andhra Pradesh 517506, India

ARTICLE INFO

*Keywords:*
4H-silicon carbide
Electrical characteristics
Schottky barrier diode
Thermal annealing
Traps
Thermally stimulated capacitance

ABSTRACT

Thermal annealing effects on electrical characteristics of Ni/4H-SiC and Ti/4H-SiC Schottky barrier diodes (SBDs) are investigated in the temperature range of 400–1100 °C. The thermal evolution of deep level traps in annealed SBDs is also analyzed by thermally stimulated capacitance (TSCAP) spectroscopy. As-deposited Ni/4H-SiC SBDs exhibited non-ideal electrical properties compared to Ti/4H-SiC SBDs. The electrical parameters of the Ni/4H-SiC SBDs are improved upon annealing at 400 °C for 30 min. in Ar ambient. However, deterioration in the SBD characteristics is observed from the temperature of 500 °C, so optimal annealing temperature for our Ni/4H-SiC SBDs is 400 °C. On the other hand, electrical properties of the Ti/4H-SiC SBDs are found to degrade even from the annealing temperature of 400 °C and hence as-deposited Ti/4H-SiC SBDs have the better properties. No considerable changes in the trap concentrations at $E_c$-0.63 eV and $E_c$-1.13 eV are identified in the SBDs up to the annealing temperature of 600 °C. The heat treatment on or above 800 °C results in poor rectifying behavior in both the SBDs, therefore the diode rectification is disappeared from 800 °C.

## 1. Introduction

Epitaxial 4H-silicon carbide (4H-SiC) Schottky barrier diodes (SBDs) are recommended for high-power electronic systems [1, 2], high-temperature applications [3], and radiation detection in hostile environments [4, 5]. For the possible use in these applications, the electrical properties of the 4H-SiC SBDs need to be optimized and improved. As deposited 4H-SiC SBDs may exhibit non-ideal electrical characteristics [6–9]. The electrical parameters of the SBDs can be improved by thermal annealing [10–16]. Among the metals suitable for contacts, Ni and Ti are preferred for Schottky contact on n-type epitaxial 4H-SiC [6–17]. The low work function of the Ti (unlike Ni) allows the formation of Ohmic contact on highly doped ($> 10^{18}\,cm^{-3}$) n-type 4H-SiC substrate with a low specific contact resistivity (SCR) of $2.25 \times 10^{-3}\,\Omega$-$cm^2$ [18] without any heat treatment [10, 19]. Hence, two types of SBDs such as Ni/4H-SiC SBDs and Ti/4H-SiC SBDs (Ti/Au bimetal layer Schottky contact) are fabricated in this work, with the Ti/Au bilayer as an Ohmic contact for both the SBDs.

Many authors investigated the thermal annealing induced changes in the electrical characteristics of Ni/4H-SiC and Ti/4H-SiC SBDs with Ni as back Ohmic contact [11, 12, 15, 16, 20–27]. Whereas, limited reports are available for heat treatment effects on 4H-SiC SBDs with the Ti Ohmic contact [10, 13, 14, 17, 19]. Kestle et al. [10] obtained an improved electrical performance at an annealing temperature of 500 °C for Ni/4H-SiC/Ti SBDs; but the authors observed poor rectifying nature at 600 °C. Vacuum annealed Ni/4H-SiC/(Ti/Ni/Ti) SBDs have shown [13] better Schottky barrier properties at the temperature of 500 °C. Zaman et al. [19] investigated the thermal annealing impacts on Ni/4H-SiC/(Ti/Ni/Ag) SBDs in the temperature range of 600 °C to 800 °C; the authors identified degradation in the diode rectifying behavior even at the annealing temperature of 600 °C. The Ni/4H-SiC SBDs and Ti/4H-SiC SBDs used in this work have the physical structure of Ni/4H-SiC/(Ti/Au) and (Ti/Au)/4H-SiC/(Ti/Au). Gupta et al. [14, 17] reported an improvement in the electrical characteristics of Ni/4H-SiC/(Ti/Pt/Au) SBDs upon annealing at 400 °C for 30 min in Ar ambient. Since our Ni/4H-SiC SBD structure is similar to Gupta et al. [14, 17], the same annealing parameters (30 min annealing in Ar ambient) are considered and the 400 °C is chosen as the lower limit for the annealing study. It is reported that Ni can form an Ohmic contact even with the lightly doped ($\sim 4 \times 10^{15}\,cm^{-3}$) n-type 4H-SiC around the annealing temperature of 950 °C [28–30]. Hence, annealing studies are carried out up to an elevated temperature of 1100 °C. The current work may be helpful in determining the optimal annealing temperature of similar kinds of SBD structures and to understand the annealing effects on their electrical characteristics over wide temperature range than studied so far.

The SBD characteristics not only depend on the metal/

* Corresponding author.
*E-mail address:* nnmurty@iittp.ac.in (N.V.L. Narasimha Murty).

https://doi.org/10.1016/j.microrel.2018.06.021
Received 17 January 2018; Received in revised form 25 May 2018; Accepted 25 June 2018

semiconductor interface properties, but also on the electrically active defects present in the SBDs [1, 4, 5, 8]. The thermal evolution of electrically active defects in the 4H-SiC SBDs has been studied by deep-level transient spectroscopy (DLTS) [31, 32]. Storasta et al. [31] analyzed the high-temperature annealing (1600–1800 °C) effect on $Z_{1/2}$ defect in Ni/4H-SiC/Al SBDs. Recently, Mannan et al. [32] reported the thermal annealing (100 °C to 800 °C) of deep level defects in Ni/4H-SiC/Ni SBDs for the annealing time of 30 min. In the above works, the contacts were formed only after the annealing process. Therefore, the current work is focused to analyze the thermal evolution of the trap signatures in the fabricated SBDs (i.e. after the contact formations) for the further improvement of the SBD characteristics. Thermally stimulated capacitance (TSCAP) spectroscopy [33–36], an irreversible single-shot capacitance transient technique, has been used [37] to identify the traps in the 4H-SiC SBDs. The attractive feature of the TSCAP compared to DLTS is the simple measurement setup. Furthermore, alike DLTS, the TSCAP is suitable to determine the type of defects (electron/hole trap) in the sample and the signal sensitivity is independent of the device leakage current. The changes in the trap concentrations are examined after annealing by using TSCAP.

## 2. Experiment

The SBDs were fabricated on 30 μm thick n-type epitaxial 4H-SiC substrate (epilayer doping $5 \times 10^{14}\,cm^{-3}$) from CREE Inc. The 4H-SiC SBD fabrication process steps are explained elsewhere [4, 5, 37]. In Ni/4H-SiC SBDs, Ni was considered as Schottky contact on Si-face and bimetal layer Ti (50 nm)/Au (150 nm) was used as Ohmic contact on C-face. On the other hand, in Ti/4H-SiC SBDs, the Ti (50 nm)/Au (150 nm) bilayer was chosen for the Schottky and Ohmic contacts. Both the SBDs were unterminated and unpassivated. The samples were not undergone any heat treatment after the contact formations. The active area of the studied SBDs was 3.8 $mm^2$.

### 2.1. Electrical and TSCAP measurements

Initially, I-V and C-V characteristics of the SBDs were measured at room temperature. The TSCAP measurements [37] were carried out in the temperature range of 150–650 K by using the Janis® cryogenic probe station. For acquiring the TSCAP spectrum, at first, the device under test (DUT) was cooled down to a low temperature of ~150 K ($T_0$) with or without the bias voltage of −40 V. Afterwards, the trap levels in the DUT were populated by forward biasing the SBD (with a current of 2 mA) for 100 s at $T_0$. At last, the DUT was heated at a heating rate of 0.12 K/s under −40 V bias voltage from the $T_0$ and changes in the DUT capacitance vs. DUT temperature (i.e. TSCAP spectrum) were recorded in the LabVIEW interfaced NI-PXI 1031 system. During the TSCAP scan, the SBD depletion capacitance was measured at 1 MHz frequency and with a 30 mV AC signal by using Agilent 4285A LCR meter and the DUT temperature was monitored by the Lakeshore 336 temperature controller.

### 2.2. Thermal annealing process details

The thermal annealing of SBDs was performed in the temperature range of 400 °C to 1100 °C with a step of 100 °C by using CARBOLITE GERO tube furnace (STF 16/450). The samples were loaded into the furnace from the room temperature to a particular annealing temperature, and then samples were annealed for 30 min in Ar atmosphere. After the heat treatment, the samples were unloaded from the furnace and were cooled under normal ambient conditions for 30 min. Subsequently, the electrical and TSCAP measurements were conducted.

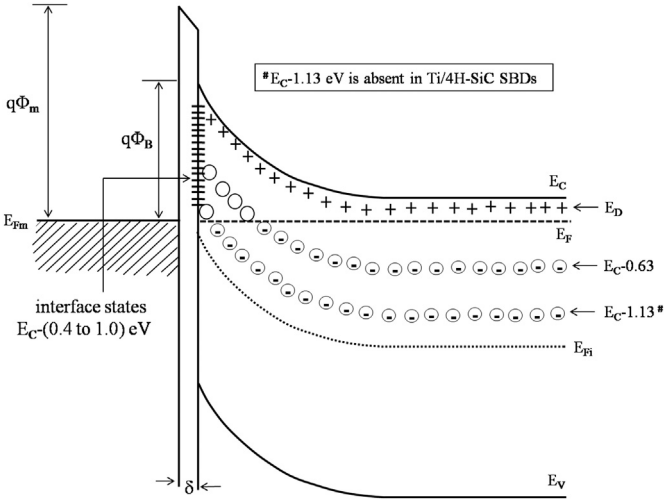


**Fig. 1.** The energy band diagram of 4H-SiC Schottky barrier diode with a thin interfacial oxide layer (δ) under equilibrium condition; the figure also displays the energy location of the deep level traps ($E_C$-0.63 eV and $E_C$-1.13 eV) in the 4H-SiC epitaxial layer and the energy level distribution ($E_C$-0.4 eV to $E_C$-1.0 eV) of the interface states at the metal/4H-SiC.

## 3. Results and discussion

### 3.1. As-deposited SBD characteristics

Electrically active defects (traps) in the SBDs identified by the TSCAP spectroscopy are reported elsewhere [37] and are summarized: Two deep traps such as P1 ($E_C$-0.63 eV, $Z_{1/2}$) and P2 ($E_C$-1.13 eV, EH5) are identified in the Ni/4H-SiC SBDs with a trap concentration of $\sim 7 \times 10^{12}\,cm^{-3}$ and $\sim 1.3 \times 10^{13}\,cm^{-3}$. It should be noted that the trap P2 (EH5) is detected in the TSCAP spectrum for the DUT cooling procedure carried out with and without bias voltage. Thus, the trap P2 does not exhibit the metastable nature of the EH5 defect reported in the literature [38, 39]. While, a single trap level P1 is found in the Ti/4H-SiC SBDs with the trap density of $\sim 6 \times 10^{12}\,cm^{-3}$. The trap P2 is not observed in the TSCAP spectrum for both the cooling conditions revealing that the P2 is absent in the Ti/4H-SiC SBDs. Fig. 1 shows the energy band diagram of the 4H-SiC Schottky barrier diode with a thin interfacial oxide layer (δ) under thermal equilibrium condition; the figure also displays the energy location of the deep level traps ($E_C$-0.63 eV and $E_C$-1.13 eV) in the 4H-SiC epitaxial layer and the energy level distribution ($E_C$-0.4 eV to $E_C$-1.0 eV) of the interface states at the metal/4H-SiC. The energy band diagram of the Ti/4H-SiC SBD also looks similar to the Fig. 1, except the absence the deep trap level $E_C$-1.13 eV.

Fig. 2 shows the forward current-voltage ($I_F$-$V_F$) characteristics of as-deposited Ni/4H-SiC SBDs along with the $I_F$-$V_F$ at the annealing temperature of 400 °C (discussed later) and the inset displays the pre-annealing reverse current-voltage ($I_R$-$V_R$) plot. The forward voltage drop across the SBD at 1 mA is obtained as ~1.5 V. Two linear regions noticed in the semi-log $I_F$-$V_F$ characteristics indicating the existence of inhomogeneous Schottky barrier height (SBH) at the Ni/4H-SiC interface associated with two distinct SBHs [6, 40, 41]. The SBH ($\Phi_B$) is calculated by using the following expression [14, 17, 42]

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_S}\right) \quad (1)$$

where $k$ is the Boltzmann's constant, $T$ is the temperature, $q$ is the elementary charge, $A^*$ is the effective Richardson constant for n-type 4H-SiC ($146\,A\,cm^{-2}\,K^{-2}$) [14, 17, 43], and $J_S$ is the reverse saturation current density ($J_S$) extracted from the linear region of $\ln(J_F) - V_F$ characteristics. The SBH for linear-1 and linear-2 regions is found to be