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Review paper

Identification of oxide defects in semiconductor devices: A systematic approach linking DFT to rate equations and experimental evidence

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ABSTRACT

It is well-established that oxide defects adversely affect functionality and reliability of a wide range of microelectronic devices. In semiconductor-insulator systems, insulator defects can capture or emit charge carriers from/to the semiconductor. These defects feature several stable configurations, which may have profound implications for the rates of the charge capture and emission processes. Recently, these complex capture/emission events have been investigated experimentally in considerable detail in Si/SiO_2 devices, but their theoretical understanding still remains vague. In this paper we discuss in detail how the capture/emission processes can be simulated using the theoretical methods developed for calculating rates of charge transfer reactions between molecules and in electro-chemistry. By employing this theoretical framework we link the atomistic defect configurations to known trapping model parameters (e.g. trap levels) as well as measured capture/emission times in Si/SiO_2 devices. Using density functional theory (DFT) calculations, we investigate possible atomistic configurations for various defects in amorphous (a)-SiO_2 implicated in being involved in the degradation of microelectronic devices. These include the oxygen vacancy and hydrogen bridge as well as the recently proposed hydroxyl E' center. In order to capture the effects of statistical defect-to-defect variations that are inevitably present in amorphous insulators, we analyze a large ensemble of defects both experimentally and theoretically. This large-scale investigation allows us to prioritize the candidates from our defect list based on their trap parameter distributions. For example, we can rule out the E' center as a possible candidate. In addition, we establish realistic ranges for the trap parameters, which are useful for model calibration and increase the credibility of simulation results by avoiding artificial solutions. Furthermore, we address the effect of nuclear tunneling, which is involved according to the theory of charge transfer reactions. Based on our DFT results, we demonstrate the impact of nuclear tunneling on the capture/emission process, including their temperature and field dependence, and also give estimates for this effect in Si/SiO_2 devices.

1. Introduction

Metal-oxide-semiconductor transistors are used in a wide range of electronic devices underpinning 'internet of things' and most technologies and therefore have become an indispensable part of our daily lives. Their technological success has been the result of intensive R&D efforts, which have continued over decades and led to substantial changes in technologies used for producing these devices. Nevertheless, the technologically most relevant field-effect transistors (FETs) are still based on semiconductor-insulator interface systems which are required for the field-effect and thus the functionality of the transistors. While idealized materials can be assumed for the basic understanding of their functional principles, real devices contain defects, particularly in the amorphous insulator and its interface to the semiconducting channel. For instance, P_b centers, three-coordinated Si atoms with a dangling bond, have been detected at Si/SiO_2 interfaces by electron spin resonance (ESR) spectroscopy [1,2]. In SiO_2, this measurement method revealed the existence of several types of so called E' centers [1,2], which originate from Si dangling bonds. Among them, the most prominent are variants of the E'_γ center usually associated with oxygen deficiency. In addition, the 74 and 10.4 G doublet center, hydrogenated variants of the E' center, have been discovered in SiO_2[3]. The existence of these ESR-active centers has also been confirmed by spin-dependent recombination experiments (SDR) [4]. Furthermore, investigations based on spin dependent tunneling (SDT) have revealed the existence of K_n centers in nitrided oxides [5].

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In numerous electrical measurements, defects have been demonstrated to be electrically active, meaning that they can capture and emit charge carriers from the substrate as well as the gate. These defects, commonly referred to as charge traps, can strongly affect the device characteristics or even impair the functionality of the transistors. For instance, they were suggested to be involved in time-dependent dielectric breakdown, causing device failure [6]. There are other prominent and serious issues, such as stress-induced leakage currents (SILC) [7–9], random-telegraph noise (RTN) in the drain current [10], bias temperature instability (BTI) [11]. These phenomena have not only been observed in conventional Si-based transistors but also in other important technologies: In SiC and GaN power devices, charge capture and emission were found to occur in such large concentrations that they dominate the device functionality [12,13]. Furthermore, the introduction of novel two-dimensional materials is expected to provide high device performance in terms of switching speed and power consumption but has already been shown to suffer from charge trapping too. As such, charge trapping appears to be a widespread issue among all transistor technologies [14,15].

For decades, these charge trapping phenomena have been investigated by different experimental techniques: For instance, RTN measurements and time-dependent defect spectroscopy (TDDS) can be used to detect single charge trapping events of selected defects and provide insight into the mechanisms behind charge trapping. Other measurement techniques are $I_d(V_g)$ measurements [16–19], charge pumping [20,21], measure-stress-measure [22–25], and on-the-fly measurements [26,27] among others. However, all of them have initially been designed for large-area devices, in which a multitude of charge trapping events superimpose and thus single defects cannot be assessed experimentally.

In all these measurement techniques, charge trapping essentially occurs for two distinct operation modes of the transistors: In one mode, the gate bias is kept at a constant level and the charge capture and emission events occur stochastically distributed in time and give rise to drain current noise for instance. As such, an RTN signal corresponds to the equilibrium response for this operation mode with regard to charge trapping. In the other mode, the transistor is alternatingly operated at a high and a low gate bias level, where the former typically accelerates capture events while the latter accelerates emission. The acceleration due to the applied bias has motivated the term ‘stimulated charge trapping’ for this operation mode and will be used throughout this paper.

In order to better describe these phenomena theoretically, several models have been put forward. In those models, the charge trapping process has often been treated using phenomenological approaches [28] for calculating the capture and emission rates. More sophisticated models [29,30] already accounted for the tunneling of charge carriers through the energy barrier from the substrate into the trap or vice versa. McWorther et al. [31–33] incorporated the tunneling effect into the Shockley-Read-Hall (SRH) theory in order to account for the broadly distributed capture/emission (C/E) times via a different trap depth. Kirton et al. [10] observed a strong temperature dependence of the C/E time constants in the measured drain current noise. In order to explain this, he also gave the capture/emission (C/E) process a first microscopical interpretation within the framework of the nonradiative multi-phonon (NMP) theory. This finding implied that the established SRH model is an oversimplifying description for C/E processes and is not applicable to charge trapping in oxide defects [34].

Even though some variants of the NMP theory have been applied in several studies [8,35-38], their physical formulations often rely on simplifying assumptions. Most of them are based on a model Hamiltonian in which the interactions between the electrons and the phonons are described by a single term. As an approximation, this term is expanded in a series of the atomic coordinates **R** and assumed to be dominated by the first or second order term, referred to as ‘linear’ or ‘quadratic’ electron-phonon coupling, respectively. Although this approach allows for closed-form expressions of the nonradiative multi-phonon transitions, it does not capture the full complexity of actual charge capture or emission processes.

Similar processes have been thoroughly investigated under the term ‘charge transfer’ (CT) reactions in the context of chemistry [39]. These reactions are well described by a variety of theories, which have been developed at various levels of sophistication. The most popular formulation was proposed by Marcus, who was awarded the Nobel prize in chemistry for his pioneering work in 1992. Meanwhile, these theories have become well-established in many fields of chemistry and biology and are routinely used to describe processes, such as photosynthesis, corrosion, and chemiluminescence. Even though these theories led to a significant progress in the understanding of molecular conduction in nanoelectronics [40,41], they have remained virtually unrecognized in the microelectronics community. In principle, the theory of CT reactions already lays the foundation for modeling the actual C/E processes involved in charge trapping. Defect model must still be adapted to the case of microelectronic transistors where semiconductor-insulator material systems are encountered. This requires consideration of all interactions with the band states in the semiconductor substrate and the gate contact, as it has already been done for molecular conduction [40,41]. Furthermore, such a model must also account for the presence of additional defect states as suggested by various measurements [42,43].

In order to gain an atomistic insight into charge trapping, the defects in the dielectrics were also investigated theoretically in numerous density functional theory (DFT) studies [44]. For instance, the P_b center has been intensively examined [45] and its reactions with atomic and molecular hydrogen considered in [46,47]. Furthermore, the positively charged oxygen vacancy in SiO_2 was found to be stable in two configurations where one of them could be related to the E' center [48–50]. The property of having two stable configurations is also referred to as ‘bistability’ and maybe linked to some unexpected behavior of defects in microelectronic transistors. As such, it was the subject of intensive discussions but has been confirmed by several independent groups [49–55]. From a device perspective, it has been shown that the oxygen vacancy easily reacts with a hydrogen and forms a defect called hydrogen bridge [7,56], which has a defect level within the SiO_2 bandgap. In a number of publications [44,57-59], several other defects have been found to introduce trap levels within the HfO_2 bandgap. Furthermore, possible bistable defect configurations were proposed by Joeng et al. [60] for nitrided oxides. In all those studies, however, the results of DFT calculations were not used to predict the electron capture and emission rates. In this paper we attempt to provide a link between the electronic properties of defects in the oxide and electron C/E rates measured experimentally.

To achieve that, we first present a rigorous derivation of a defect model to describe the various aspects of charge trapping and to link its parameters to atomistic simulations. To provide the experimental foundations, the findings from TDDS studies will be summarized and their implications for the defect model discussed in Section 2. Next, the transition rates of C/E processes will be formulated based on the theory developed for CT reactions (in Section 3). The resulting rate expressions will then be incorporated in the defect model suggested by TDDS experiments. Section 5 is devoted to defects which have been associated with charge trapping phenomena and investigated by DFT. In Section 6, their potential energy surfaces will be studied and related to the parameters of the defect model.

2. Findings from TDDS studies

Recently a new measurement technique, termed TDDS, has shed additional light on charge trapping in microelectronic transistors [61,62]. It makes use of the fact that single charge capture/emission events in small-area devices can be resolved as discrete steps in the drain current or the threshold voltage. The step heights in combination