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Sub-1 ns characterization methodology for transistor electrical parameter extraction

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ABSTRACT

In this paper, a novel method is proposed for the extraction of the transistor electrical parameters at the nanosecond timescale. This technique is enabled by an ultra-fast measurement (UFM) system that mainly contains the arbitrary waveform generator and a high-speed real-time oscilloscope. De-noising, synchronization and calibration problems are solved to improve the accuracy and precision. To circumvent the circuit problem at the drain of the transistors, a three-dimensional (3-D) I-V characterization solution is reported, and the I_D-V_G and I_D-V_D measured at sub-1 ns time are then drawn. The I-V curves measured in 800 ps show unprecedented agreement with that measured by a standard parameter analyzer and can be used for device/circuit modeling and reliability behaviors studies.

1. Introduction

With the wide application of Internet of Things and Big Data, the computing speed of CPUs is becoming increasingly important because it plays one of the most significant roles in determining the performance of various integrated circuit systems. As the basic component of CPUs, transistors have been shrinking following Moore's Law while their switching speed has been increasing exponentially [1]. Fig. 1 shows the clock frequency evolution for four main microprocessor manufactures and some other brands in history [2]. It is clear that the clock frequency of mainstream microprocessors approached the gigahertz range years ago, that is to say, the switching time of the transistors in the microprocessor should be < 1 ns. However, commercial semiconductor parameter analyzers require at least hundreds of nanoseconds for the characterization of electronic properties so that many faster transient phenomena could not be observed. To obtain the 'real' transistor model under the circuit speed operation, ultra-fast (sub-1 ns) device characterization techniques are necessary.

On the other hand, FinFET and SOI device structures have been adopted by industry for suppressing the leakage current and short channel effects. However, due to the low thermal conductivity of the buried oxide and the physical confinement of the silicon fin, both structures suffer from significant self-heating effects (SHE) that lead to performance and reliability degradation [3–6]. Since thermal generation and dissipation are time-consuming, in order to evaluate the SHE, speed-variant measurements are necessary to understand the impact of the SHE on device operation in real circuits. However, the conventional characterization setups can only perform one type of measurement (e.g., I_D-V_G or I_D-V_D) in microseconds or hundred seconds, which is much slower than the circuit speed and therefore cannot be used to capture the SHE properly.

In terms of device reliability behaviors, negative bias temperature instability (NBTI) is the most elusive phenomenon, and because of its recovery nature, the physical mechanism of NBTI is not well understood. The key challenge is the short recovery process (within sub-10 ns), which is orders of magnitude faster than the current characterization speed. Tremendous efforts have been made to solve this problem, for example, the fast I-V testing method similar to the on-the-fly technique has been introduced to bridge the timescales. However, the measurement speed of this technique is still at the level of 100 ns [7–10]. In addition, ultra-fast measurements are also necessary for another important reliability phenomenon, hot carrier injection (HCI), to eliminate the effect of SHE on the HCI-induced device degradation. Otherwise, the HCI-induced degradation may be overestimated [11]–[12]. As shown in Fig. 2, available current and impedance measurements require hundreds of nanoseconds or more. Therefore, faster measurement speed is absolutely required to relieve this inadequacy, not only for the 'real' circuit parameter extraction but also for a series of mechanism effects, such as self-heating, HCI and BTI. Additionally, increased measurement speed can also help the improvement of productivity from an engineering point of view.

In this study, we propose an ultra-fast device characterization

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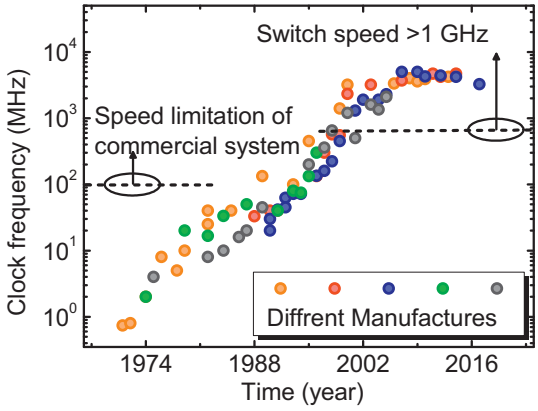

Fig. 1. Development of clock frequency and device clock frequency in mainstream CPU [2] and the comparison of commercial device performance measurement speed and switching speed in 'real' circuits.

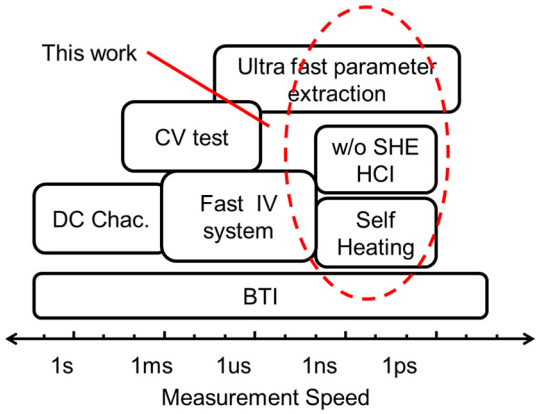

Fig. 2. Device measurement speed and its application to different reliability issues. It is clear that many reliability behaviors could be well-studied with this characterization technique.

technique that could be applied for sub-1 ns I-V characterization. This paper is organized as follows. In section II, the experimental setup for our ultra-fast characterization technique is described. In Section III, the measurement procedure for sub-ns characterization is outlined, and three-dimension I-V methodology is discussed. The corresponding results measured in 1 μs and sub-1 ns are shown as well. Conclusions are finally drawn in Section IV. Device characterization techniques are critical for the precise extraction of device parameters that are absolutely required for device/circuit modeling and reliability behaviors studies. Using this newly developed technique, sub-1 ns electronic properties can be directly measured for much more accurate parameter extraction.

2. Ultra-fast measurement system

Normally, device's parameter extraction for devices is performed by commercial semiconductor parameter analyzer equipped with the source measurement unit (SMU) or waveform generator/fast measurement unit (WGFMU). The A/D converters in the above units require at least hundreds of nanoseconds for integration operation in order to obtain precise results. To study transient device behaviors and their underlying physical mechanisms, some researchers developed their own in-house systems, mainly comprising a pulse generator and oscilloscope [9–12,15].

The sub-1 ns characterization technique is performed using the ultra-fast measurement system. An example of the transistor characterization is schematically shown in Fig. 3(a). The gate bias V_G is

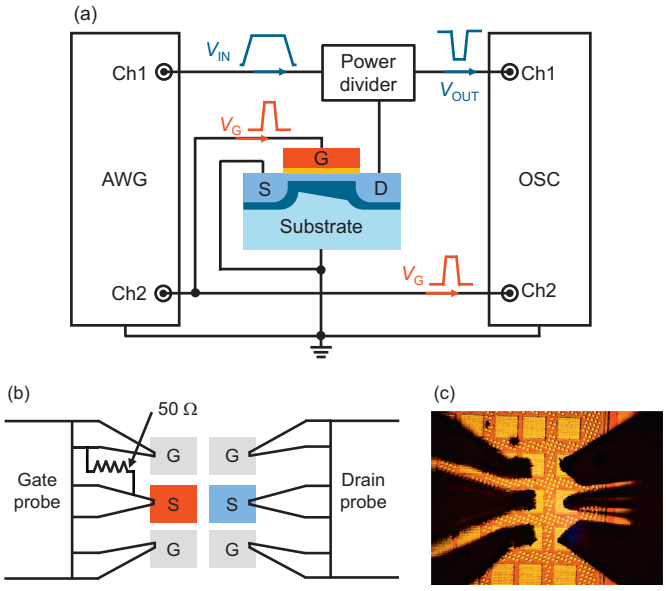

Fig. 3. (a) Schematic of the proposed ultra-fast I-V measurement system using AWG and OSC. (b) Schematic diagram of gate probe, which has the customized 50 Ω impedance terminated and the other normal GSG probe at the drain. (c) Photo of GSG RF probes and RF electrode patterned transistors obtained using an optical microscope.

supplied by a commercially available arbitrary waveform generator (AWG) via a customized ground-signal-ground (GSG) RF probe with 50 Ω termination (Fig. 3(b)), which aims for the impedance matching. Another normal GSG RF probe connects to the drain of the transistor for drain voltage V_D supply and drain current I_D acquisition. The AWG supply the drain pulses via the other channel. The high-speed real-time oscilloscope (OSC) is equipped to sense the tiny real time change of the I_D, represented as V_{OUT} on the OSC. A power divider provides a method to carry out these two measurements simultaneously without sacrificing the high-speed signal integrity. Notably, the high-level time in each drain pulse should be longer than that of the gate pulse for the transistor operation. The AWG has a sample rate of 50 GS/s. The OSC has a real-time sample rate of 100 GS/s and a max record length of 1G points. Subtle calibration and synchronization between AWG and OSC have been carried out carefully to ensure the minimization of parasitic effects, as will be shown in section III. Fig. 3(c) presents the image of the transistor pads with the GSG structure and the RF probe at each side. SMA cables are used to transport high-frequency signal in this system. The outer shield of AWG, OSC and probe station is all connected to the same ground.

3. Characterization technique and result

To accomplish the sub-ns I-V characterization of transistors, four key problems must be solved: 1) the first problem is the noise suppression that directly determines the precision of the result. The noise sources in our study are due to the high-frequency measurements and unknown effects from the environment. 2) The V_G signal should be time-synchronized with the V_{OUT} signal, or else the mismatch time sequencing will cause the wrong congruent relationship between V_G and I_D to be calculated by V_{OUT}. 3) The AC/DC agreement, which means that the I-V curves measured by UFM system, should be in agreement with that measured by standard parameter analyzer, or else an incorrect amplitude will be caused by the resistors in power divider. 4) Last but not the least, the V_D (V_G) should be strictly the same in the final I_D-V_G (I_D-V_D) curves, which is difficult to obtain in high-speed characterization. In conclusion, the entire measurement procedure (Fig. 4) of the ultra-fast measurement technique is composed of four main steps: