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Effect of aging on mechanical properties of high temperature Pb-rich solder joints

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ABSTRACT

The effect of aging on the evolution of interfacial microstructure and mechanical properties of Pb-rich PbSnAg solder joints with different Sn content was investigated. Tensile samples were prepared by soldering two pieces of Ni or Cu strips resulting in joints with gap sizes of about 250 µm. Multi-layered structures composed of Ni coated Si-chips soldered onto Ni/Cu metallized ceramic substrates were used for fatigue testing. All samples were subjected to thermal aging at 250 °C up to 500 h. Microstructural investigations revealed that independent from the substrate material, increased Sn content of the solder alloy results in improvement of the tensile and fatigue properties of the joints and a higher growth rate of the interfacial intermetallic compound (IMC) layers. It was found that the thickness of the wettable substrate especially in the case of low-Sn alloys, also affects the interfacial properties of high temperature PbSnAg solder joints. In this case, a reduced Sn content in solder joints results in weakening of the interface during the reflow process and subsequent thermal aging. The dominant failure mode of the solder joints subjected to cyclic loading was delamination of the interfacial IMC layer from the substrate. Finite element simulations were conducted by using a strain rate and pressure dependent material model for PbSnAg solder in order to analyse the states of stress and strain during static and cyclic loading.

1. Introduction

Lead rich Pb-Sn solders with additions of Ag are used for die attach applications in high power semiconductor devices with high level of reliability requirements. While the ongoing research and development activities for implementation of alternative and new bonding solutions including Ag-sintering, low temperature transient liquid phase sintering (e.g. Cu and Sn) or high melting Pb-free solders are promising, high temperature Pb-solders are still exempted from RoHS regulations [1,2]. Due to the limited available data on their long term reliability, the alternative technologies have not been yet established as adequate replacements for high-Pb solders [2,3]. Typical compositions of the Pb-rich, binary PbSn and ternary PbSnAg solders with melting points in the range of 300 °C and above, include 5 to 15 wt% tin and up to 5 wt% silver. For many years, Pb-rich solders have been used in flip chip technology and die attach applications due to their microstructural stability, slow growth rate of the interfacial IMCs and thermo-mechanical fatigue resistance in combination with reasonable costs. Besides these beneficial properties, a drawback of the lead rich PbSn solders is the possible occurrence of large scale delamination of the IMC layer from the interface during the soldering or subsequent aging [4,5] This behaviour has been found to be particularly dependent on the amount of the reactive constituent element of the solder. Spalling phenomena have also been observed in several lead-free Sn-based metallurgical systems such as Sn-Cu-Ag, Sn-Zn on Cu or Ni substrates [4–8]. Several studies show that not only the composition of the diffusion pair may affect the morphology and growth rate of the interfacial IMC layers in PbSn solder joints, but also the thickness of the wettable substrate and the joint. Moreover, processing parameters like reflow time and temperature are important factors [4,8,12,13].

In semiconductor devices, the solder joints between the die and the substrate and the substrate and base plate are subjected to thermal and mechanical stresses during the processing and subsequent operation. The solder die attach is regarded as one of the most critical sites in high temperature power modules [9,10]. Presence of temperature gradients during the service and mismatch of the coefficient of thermal expansion (CTE) of the neighbouring materials results in thermo-mechanically induced stresses in the soldered layers of the devices. During the service, cyclic plastic deformation, gradual microstructural changes and growth of the intermetallic layers can result in degradation of the solder joints and final failure of the devices [10–12]. The reliability of semiconductor devices is conventionally determined by active or passive

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thermal cycling tests [10]. Accelerated mechanical fatigue testing has been proposed as an alternative technique for rapid evaluation of various interconnects. Besides the time saving factor, this technique allows separate investigation of different thermomechanically induced failure modes in the devices [14]. Recently high frequency isothermal bending fatigue testing has been introduced for accelerated lifetime assessment and rapid evaluation of die attach or other large area joints in semiconductors [15]. In the present work the effect of aging on the tensile properties and fatigue response of high-lead PbSnAg die attach solders used in high power electronics has been studied. Tensile tests and accelerated cyclic bending experiments were conducted on model solder joints which were prepared by using two types of alloys with different Sn content and Cu or Ni substrates. All samples were subjected to thermal aging in order to study the effect of morphology, growth rate and possible spalling of the IMC layers on the mechanical response of the solder joints. Finite element simulations were conducted to analyse the state of thermal and mechanical stresses and strains in the samples during static and high frequency cyclic loading. A modified Anand model was used in order to consider the temperature and strain rate effects as well as pressure dependence of plasticity in the solder joints.

2. Sample preparation and experimental setups

Solder joints for tensile testing were prepared by using Cu and Ni strips of 99.9% purity and two types of PbSnAg solder alloys (Pb > 85 wt%) with lower and higher Sn content, hereafter named as PbSnAg-1 and PbSnAg-2, respectively. The butt joints were prepared by using pairs of Cu and Ni strips with cross sections of 2 × 3 mm and lengths of 20 mm. Each pair was put and aligned in an adjustable soldering jig with the distance between the two pieces being 250 μm. Thin solder foils were placed between the two strips resulting in joints with almost similar gap size of 250–300 μm after the reflow process (Fig. 1a). The excessive solder layers on the free surfaces of the reflowed samples were removed by fine mechanical polishing. The samples were subsequently aged at 250 °C for time intervals of 48, 115, 250 and 500 h in air. A commercial micro-tensile machine with a load cell capacity of 500 N was used for tensile experiments. The solder joints with a gauge length of 20 mm were tested at a constant strain rate of about $5e-4\,s^{-1}$.

For bending fatigue experiments, commercial IGBT-chips with Ni back side metallization of 1 μm were soldered onto the Ni coated Cu layer of ceramic substrates by using the two types PbSnAg solders. The thickness of solder die attach was in the range of 90 to 140 μm and the dimensions of the substrate were 15 × 27 mm. In order to avoid cracking and fracture of the ceramic substrate during the three-point cyclic bending tests, a steel sheet with a thickness of 750 μm was glued at the reverse side of the substrate (Fig. 1b). The dimensions of the multi-layered fatigue samples were adjusted to provide the resonant conditions required for fatigue testing at 20 kHz. For this purpose, FEM simulations were performed to compute the natural frequencies of specimens. Samples of appropriate dimensions were subsequently subjected to thermal aging at 250 °C for 250 and 500 h in air for microstructural investigations. Fatigue tests were conducted on both series of samples in as-reflowed condition. Those prepared with a higher Sn content were also tested after aging at 250 °C for 250 h.

An ultrasonic resonance testing system operating at a frequency of 20 kHz equipped with a 3-point bending stage was used for cyclic bending experiments. The resonant sample is placed on the two cylindrical supports of a bending stage below the half cylindrical shaped tip of the acoustic horn. During the fatigue loading, the tip is pressed to the mid-section of the sample with a slight pre-load and the sample is excited to transversal vibrations. The failure criteria for lifetime measurements were defined as separation of the chip from the substrate due to delamination or cracking of the solder layer or partial fracture of the chip. A picture of the ultrasonic resonance fatigue test system with a magnified image of the sample is shown in Fig. 2. For more details on the ultrasonic bending fatigue testing system we refer to [15].

Metallographic sections were prepared from the solder joints in as-reflowed and aged conditions for microstructural investigations and determination of the IMC growth rate.

3. Experimental results

3.1. Microstructural investigations

The typical microstructure of the studied PbSnAg solder joints consists of a Pb-rich solid solution matrix with precipitates of β-Sn and Ag_3Sn intermetallics and some larger grains of both phases [11,15,16]. Fig. 3a and b show the microstructure of the PbSnAg-1 die attach solder joint used in this study which is typical for both alloys. Occasionally Ag_3Sn particles with sizes exceeding several micrometres could be observed in as-reflowed joints [15]. The upper and lower inserts in Fig. 3a correspond to the microstructure of the interfacial regions next to the Ni/Si-chip and the Ni/Cu metallized ceramic substrate respectively. EDX analysis indicated formation of Ni_3Sn_2 phase at the chip/solder interface and Ni_3Sn_4 at the solder/substrate interface in as-reflowed condition for both types of die attach solder joints. According to Ni-Sn phase diagram, Ni_3Sn, Ni_3Sn_2 and Ni_3Sn_4 equilibrium phases can be formed during Sn/Ni reactions. The Ni_3Sn_4 phase has often been reported to be the primary phase which is formed at the interfaces of PbSn/Ni [4,8] and PbSnAg/Ni [17] solder joints. Ni_3Sn_2 was reported to be formed at the interface between Ni and PbSn alloys with Sn concentrations below 3% [18]. According to [19] Ni_3Sn_4 is formed at Sn/Ni interfaces at rather low temperatures, whereas Ni_3Sn and Ni_3Sn_2 are found after long time treatment at higher reaction temperatures. In fact, either phase was formed at the interface of Sn −3.5% Ag/Ni after reaction at 400 °C for 24 h.

The microstructural evolution of the die attach solders at the chip side for the two types of alloys is presented in Fig. 4. The thickness of the Ni back side metallization is < 1 μm and provides a limited source of nickel for long term solid state reactions. Fig. 4a shows that already in as-reflowed condition small voids (thin gaps) are occasionally detected between the Ni layer and the Ni_3Sn_2 IMC phase at the interface of PbSnAg-1. Annealing of the solder joints up to 250 h resulted in the growth of an inhomogeneous IMC layer which was concurrent with a partial consumption of the Ni film and detachment of the NiSn phase from the interface (Fig. 4b). The thickness of the IMC layer was measured to be in the range of about 1.5 μm and in a few cases it reached a

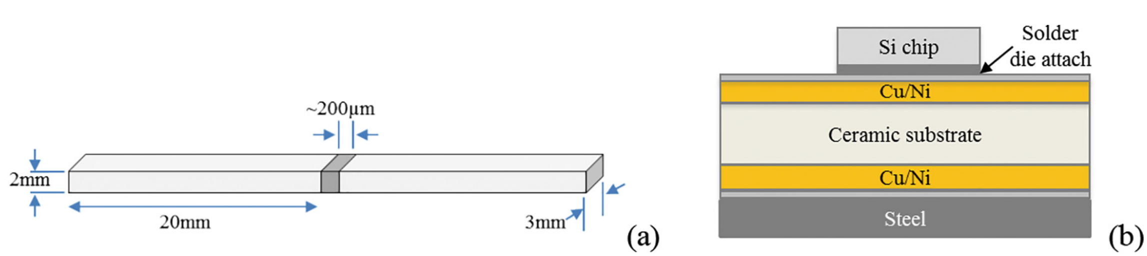

Fig. 1. Schematic images of the tensile test samples (a) and the multi-layered test structure for bending fatigue experiments (b).

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