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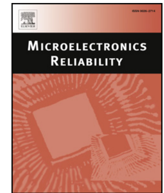
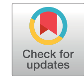


Effect of lanthanum silicate interface layer on the electrical characteristics of 4H-SiC metal-oxide-semiconductor capacitors



Y.M. Lei[a], H. Wakabayashi[a], K. Tsutsui[b], H. Iwai[b], M. Furuhashi[c], S. Tomohisa[c], S. Yamakawa[c], K. Kakushima[a,*]

[a] School of Engineering, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
[b] Institute of Innovative Research, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
[c] Advanced Technology R&D Center, Mitsubishi Electric Corporation, 8-1-1, Tsukaguchi-honmachi, Amagasaki 661-8661, Japan

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ABSTRACT

The effect of La-silicate interface layer (IL) on the electrical characteristics of 4H-SiC metal-oxide-semiconductor (MOS) capacitors with atomic-layer-deposited SiO_2 (ALD-SiO_2) gate dielectrics was investigated. In addition to a slight reduction in the interface state density (D_{it}), the surface potential fluctuation was greatly reduced due to the reduction in the fixed charges (Q_{fix}) with La-silicate IL. Moreover, two orders of magnitude reduction in the oxide trap density in the ALD-SiO_2 layer adjacent to the La-silicate IL was confirmed. Physical analysis revealed the reduction in carbon concentration and incorporation of La atoms adjacent to the La-silicate IL.

1. Introduction

Silicon carbide (SiC) is a promising candidate for next-generation power device semiconductor, owing to its wide bandgap and its high thermal conductivity [1,2]. One of the issues in 4H-SiC metal-oxide-semiconductor (MOS) field-effect transistors is that SiO_2 gate dielectrics still suffer from high interface state density (D_{it}) which causes severe degradation in the channel mobility [3]. To overcome the issues of high D_{it}, various approaches have been proposed to passivate the defects at the SiO_2/SiC interface; incorporation of nitrogen atoms by annealing in NO-based gas [4] or phosphorous atoms either by $POCl_3$ annealing [5] or by deposition of phosphosilicate glass (PSG) [6]. Although these approaches improve the channel mobility to some extent, a negative shift in the threshold voltage appears as an issue. Recently, atomic layer deposited (ALD) SiO_2 gate dielectrics with a La-silicate interface layer (IL) in combination with NO-based annealing has been reported to be effective in improving the interface properties and a channel mobility over 130 cm^2/Vs has been presented [7]. In addition, the negative shift in the threshold voltage was well suppressed. Although a detailed analysis of the La-silicate IL has been reported [8], a D_{it} over 10^{12} cm^{-2}/eV with a hysteresis over several hundred mV is still high to explain the channel mobility improvements. Therefore, the physical origin of the mobility improvements is still not clear. The purpose of this paper is to clarify the effect of La-silicate IL without NO-based annealing to interface properties of SiC MOS capacitors.

2. Device fabrication

MOS capacitors were fabricated on a 4°-off angled Si-face 4H-SiC(0001) substrate with a 10-μm-thick n-type epitaxial layer. The effective carrier density (N_d–N_a) of the epitaxial layer is 1.2×10^{15} cm^{-3}. After chemical cleaning, a 2-nm-thick La_2O_3 layer was deposited by electron beam evaporation. Then, a 50-nm-thick SiO_2 layer was deposited by ALD process using cyclic injections of tris-dimethylamino-silane (TDMAS) as a precursor and O_2 remote plasma as an oxidant. During the deposition, the sample temperature was kept at 300 °C. After the ALD process, the sample was post-deposition-annealed (PDA) in O_2 ambient at 900 °C for 30 min. La-silicate IL is formed by interface reaction between the La_2O_3 and the SiO_2 layers during the PDA process [9]. A 50-nm-thick W layer was deposited by magnetron sputtering, followed by 50-nm-thick TiN capping layer to protect the surface from oxidation. The metal layers were patterned by reactive ion etching (RIE) using Cl_2 and Ar chemistries to form gate electrodes for MOS capacitors. Backside contact was formed by thermal evaporation of a 50-nm-thick Ni layer. Post-metallization-annealing (PMA) to obtain an Ohmic contact was then carried out at 950 °C by rapid thermal annealing (RTA) in forming gas (N_2: H_2 = 97%: 3%) ambient for 20 s. For comparison, an MOS capacitor without the La-silicate IL was fabricated. A gate electrode area of 50×50 μm^2 was used to measure the capacitance-voltage (*C-V*) characteristics.

The cross-sectional transmission electron microscope (TEM) image of the capacitor with the La-silicate IL is shown in Fig. 1. A uniform 2-

* Corresponding author.
E-mail address: kakushima.k.aa@m.titech.ac.jp (K. Kakushima).

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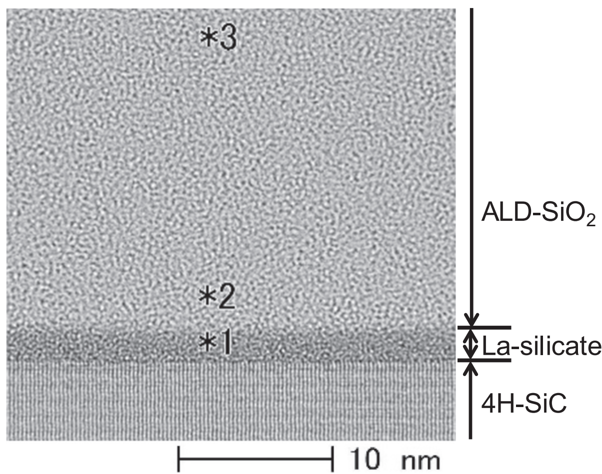

Fig. 1. Cross-sectional TEM image of MOS capacitor fabricated with La-silicate IL.

nm-thick amorphous La-silicate layer with a sharp interface to the SiC substrate can be observed. The electron energy loss spectroscopy (EELS) analysis of the La-silicate layer, marked as point 1 in Fig. 1, revealed an atomic composition to be roughly La:Si:O = 3:1:6.

3. Electrical characteristics of the MOS capacitors with La-silicate IL

3.1. Interface characteristics

Fig. 2 (a) and (b) show the *C-V* characteristics of the MOS-capacitors with and without the La-silicate IL, respectively. Firstly, both samples exhibit positively shifted *C-V* characteristics with respect to the ideal *C-V* curve calculated from the work function differences of the gate and the substrate. This fact indicates the presence of negative charges in the gate dielectrics or at the interface between the dielectrics and substrate. The difference in the depletion capacitance between the measured *C-V* and the ideal one may be reflecting the D_{it} in the midgap of 4H-SiC. The extracted equivalent oxide thickness (EOT) of the MOS capacitors with and without the La-silicate IL were 49.5 and 50.4 nm, respectively. A hysteresis in the *C-V* curve of 130 mV was enlarged to 320 mV with the presence of La-silicate IL. However, the slopes of the *C-V* curves become steeper, indicating the reduction in the D_{it}. Terman method [10] revealed D_{it} reduction from $3.4 \times 10^{12}\,cm^{-2}/eV$ to $1.6 \times 10^{12}\,cm^{-2}/eV$ at 0.24 eV away from the 4H-SiC conduction band edge (E_C) with the La-silicate IL. However, due to the detection accuracy limit of the Terman method, quantitative analysis is required to extract the D_{it} [11]. Moreover, frequency dispersions in the *C-V* curves near the flatband voltage and in the accumulation region decrease with the La-silicate IL. This fact suggests the reduction of bulk traps in the gate dielectrics [12].

The D_{it} of the capacitors was characterized by conductance method [13] under gate biases at depletion region. By using these gate biases the influence of hysteresis can be ignored and the surface potential or trap energy level can be calculated by the measured capacitance. Fig. 3 (a) and (b) show the conductance spectra (G_p/ω) of the MOS capacitor with and without the La-silicate IL, respectively. Higher peak values in the G_p/ω spectra were obtained with the La-silicate IL. However, narrower spectra with smaller full-width half-maximum (FWHM) can be observed with the La-silicate IL. Moreover, the asymmetrical shape in the spectra strongly suggests a steep change in the D_{it} within the bandgap due to the surface potential fluctuation [14]. Therefore, detailed characterization is needed to understand the interface properties. Numerical curve fitting to the obtained G_p/ω spectra based on continuum distribution of interface states [15,16], also accounting for the surface potential fluctuation with a standard deviation (σ_s) was also shown in the Fig. 3, where one can see nice reproductions for each spectrum. The extracted σ_s normalized by the thermal energy at room temperature (26 meV) and the D_{it} are shown in Fig. 4 (a) and (b), respectively. Generally, a high σ_s indicates the presence of a large amount of Q_{fix} or D_{it} at the interface [14]. Furthermore, σ_s is also influenced by the dielectric constants of semiconductor and dielectric [14]. A simple formula based on solving an electrostatic problem of a point charge at the interface between a semiconductor and a dielectric indicates that σ_s is proportional to $(\varepsilon_s + \varepsilon_{ox})^{-1}$, where ε_s and ε_{ox} are the dielectric constants of the semiconductor and the dielectric, respectively [14]. Assuming a dielectric constant of the La-silicate to be 8 [17], the σ_s of the MOS capacitor without the La-silicate IL should present a higher value by a factor of 1.3 compared to the one with the La-silicate IL. As the σ_s values revealed more than the contrast in the dielectric constants, one can conclude that the La-silicate IL can reduce the Q_{fix} or D_{it} at the interface. The D_{it} showed only a slight reduction from $8.5 \times 10^{11}\,cm^{-2}/eV$ to $7.4 \times 10^{11}\,cm^{-2}/eV$ at 0.24 eV from E_C with the La-silicate IL. Therefore, the reduction in σ_s can be mainly due to the reduction of Q_{fix} at the interface. An increasing trend in the σ_s toward the E_C of the 4H-SiC strongly suggests the interface states are mainly acceptors, in other words, positively charged when emptied [18]. Also, the D_{it} distribution shows increasing trend toward the E_C for both MOS capacitors, which is the common trend for SiO_2/4H-SiC interfaces [19]. With these analyses, the origin of the positive shift in the *C-V* curves might be the negative charges reside in the bulk SiO_2 layer.

3.2. Oxide trap density with La-silicate IL

The distribution of the oxide traps near the interface was extracted based on the model presented in refs [10,20]. Assuming oxide traps

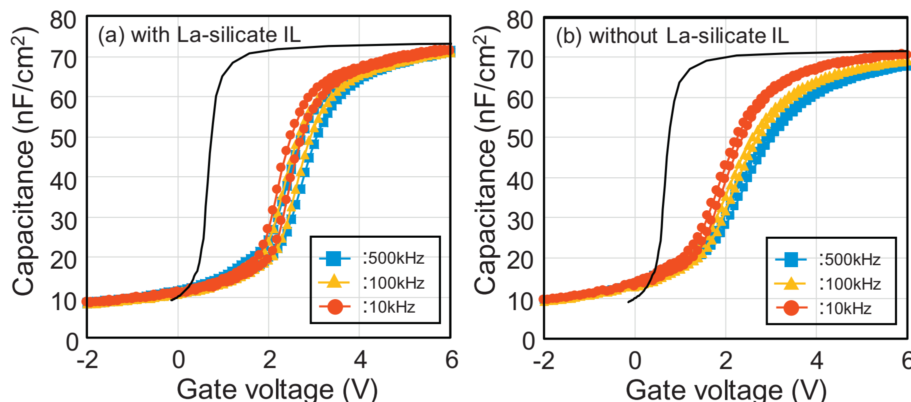

Fig. 2. *C-V* characteristics of the MOS capacitors fabricated (a) with and (b) without La-silicate IL.

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