Microelectronics Reliability 84 (2018) 1–6

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Reliability comparison of 28 V–50 V GaN-on-SiC S-band and X-band technologies

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ARTICLE INFO

Keywords:
GaN
SiC
HEMT
DC-ALT
RF-ALT
Intrinsic reliability
Wear-out

ABSTRACT

This paper discusses the reliability performance of Wolfspeed GaN/AlGaN high electron mobility transistor (HEMT) MMIC released process technologies, fabricated on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates. The intrinsic reliability performances of the 28 V and 40 V technologies, with 400 nm and 250 nm gate length, have been characterized with DC accelerated life test (DC-ALT), for which ohmic contact inter-diffusion is the wear-out mechanism, and is accelerated by temperature and current. The intrinsic reliability performance of the 50 V technologies, with 400 nm gate length, have been characterized with RF-ALT, for which source-connected second field plate void coalescence is the wear-out mechanism which is accelerated by temperature. In spite of the differences in the accelerated test methodologies and wear-out mechanisms, all of the Wolfspeed GaN-on-SiC technologies demonstrate high and similar predicted lifetimes at their respective maximum recommended operating conditions. The reliability performance is supported with successful technology qualifications with zero failures, and volume manufacturing with a demonstrated low field failure rate.

1. Introduction

This paper presents reliability results for Wolfspeed's GaN-on-SiC RF technologies. These results represent the cumulative state-of-the art knowledge collected over several years of testing, statistical analysis, and physical analysis. This paper includes new results on RF-driven accelerated life test (RF-ALT), which has very few results in the published literature. Most of the results are on DC-driven ALT, since it is much less expensive and easier to run those styles of tests. However, RF drive much more closely represents how the devices will be used in realistic applications. The results are important because of the increasingly widespread adoption of this technology for general purpose (military, civil, industrial, and scientific) and wireless (4G/5G, LTE, etc.) applications. GaN-on-SiC devices leverage the inherently robust properties of wide bandgap semiconductors to achieve higher performance, power, and junction temperature while maintaining reliability performance.

The G28 V3 intrinsic reliability performance and technology qualification on 100 mm SiC wafers were summarized by Gajewski et al., in 2011 [1]. Wolfspeed's G28 V3 and G28 V4 Title III production-capacity program and Manufacturing Readiness Level Eight (MRL8) achievement was summarized by Fury et al. in 2013 [2]. The Wolfspeed V4 technology, performance and target applications were summarized by Wood et al. in 2013 [3]. The reliability performance, including the characterization and elimination of an early life failure (ELF) mechanism that only occurs under accelerated life test (ALT) conditions, of the G40 V4 process was summarized by Gajewski et al. in 2014 [4].

2. Experimental

2.1. Device fabrication

All of the devices discussed in this paper consist of discrete high electron mobility transistor (HEMT) devices with 3.6 mm total gate periphery. The GaN-on-SiC HEMT wafers were fabricated and processed on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates with 0.40 µm (V3) and 0.25 µm (V4) gate lengths and device designs for 28 V, 40 V, and 50 V applications all of which are fully qualified and released for volume manufacturing. The devices were assembled at Wolfspeed in Research Triangle Park, NC, USA, using the production process for Cree's released product CGH40010F, a 1:1:1 CuMoCu cavity-style package with AuSn eutectic die attach, and gold wire bonds.

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https://doi.org/10.1016/j.microrel.2018.02.018
Received 20 July 2017; Received in revised form 27 January 2018; Accepted 20 February 2018

2.2. Determining junction temperature

For normal operation, qualification, and reliability tests, the channel temperature is estimated as the maximum junction temperature in the channel just under the gate corner on the drain side. Infrared (IR) microscopy and finite element analysis (FEA) are employed to produce accurate channel to case temperature differentials from which a θjc (peak junction to case thermal resistance) is calculated. An iterative process is employed, in which an IR image is taken for a given power dissipation and base plate temperature. The FEA is then spatially averaged and compared with the IR image. The thermal resistance is a modeled parameter that is adjusted iteratively until agreement is achieved between the IR and FEA. The resulting thermal resistance is then used to estimate the maximum junction temperature for a given power dissipation and case temperature, as described in [5].

2.3. Reliability testing

Intrinsic reliability tests are defined as die-level tests that are meant to stress devices under highly accelerated conditions. The goal is to determine device lifetime statistics that can be modeled to predict the device lifetime at maximum recommended operating conditions.

Extrinsic reliability qualification tests characterize the die, package, and/or die-package interaction reliability under maximum recommended normal operating conditions. The tests are meant to exercise any weaknesses or defects that may lead to early life field failures. The goal is to demonstrate product reliability with zero failures.

2.3.1. DC-ALT/high temperature operating life (HTOL)

DC-ALT/HTOL was performed under DC drive conditions at the nominal drain operating voltage (28 V, 40 V, or 50 V) and high dissipated power that is typical for many target applications (6 W/mm). The drain current was held constant throughout the test by individual gate control circuits for each device. Since all of the technologies were stressed at 6 W/mm, the higher voltage technologies encounter correspondingly lower stress current. The baseplate temperature of the thermal platform was set and actively controlled to ensure that the average device peak junction temperature target was achieved. The average peak junction temperature was estimated using thermocouples attached to the flanges of a sampling of devices and the thermal model as described above.

- DC-ALT is an intrinsic test. It was conducted by stress-measure-stress cycles, where devices were stressed for a period of time, removed from the test system for down-point test of a comprehensive suite of DC and RF device parameters at room temperature, and then the stress was continued until failure or enough degradation was achieved that the lifetime could be determined by extrapolation.
- DC-HTOL is an extrinsic test. It was run for 1000 h without interruption, followed by final test of a comprehensive suite of DC and RF device parameters at room temperature.

2.3.2. RF-ALT/high temperature operating life (HTOL)

RF-ALT/HTOL was performed under RF drive conditions at 3.5 GHz at the nominal drain operating voltage (28 V, 40 V, or 50 V) and (3–5) dB compression level. The tests were conducted using a commercial reliability test system manufactured by the Accel-RF Instruments Corporation. The devices were run at a constant input power of (26–29) dBm, which resulted in an output power of approximately 43 dBm and RF gain compression of approximately (3–5) dB. Each device fixture had its own individual heater block that actively controlled temperature in real time throughout the test to maintain a constant junction temperature as computed by the block temperature, dissipated power, and thermal model.

- RF-ALT is an intrinsic test. It was run until device parametric failure or catastrophic failure or conclusion of the test. The devices were not taken off the system for any ex-situ down points.
- RF-HTOL is an extrinsic test. It was run for 1000 h without interruption, followed by final test of a comprehensive suite of DC and RF device parameters at room temperature.

2.3.3. High temperarture reverse bias (HTRB)

HTRB testing is meant to represent continuous exposure of the die and package to the maximum recommended case temperature at worst case reverse bias pinch-off condition. The HTRB was run at 2.5–3 times the nominal operating drain voltage to simulate the maximum drain voltage that may be encountered in typical RF applications. The test is meant to exercise any high electric field failure modes and any die-level defects that may lead to early life field failures.

2.4. Device failure criteria

A device failure is defined as a condition in which a stressed device has a 1 dB change in critical RF parameters (e.g., small signal gain, saturated power (PSAT)), 20% change in saturated drain current or on-resistance, loss of pinch-off gate control, or has consequential external physical damage attributable to an environmental test. For any devices that did not reach a failure criterion by the conclusion of the ALT, their lifetimes were estimated by extrapolating the PSAT degradation to 1 dB decrease from its initial value, using an empirically-determined functional form for the time dependence.

3. Results

3.1. DC-ALT

For the DC-ALT, the RF saturated output power (PSAT) was the parameter that degraded the most significantly of all the DC and RF device parameters tested at down points. Therefore, the PSAT determines the device failure criterion and device lifetime.

3.1.1. 28 V–40 V technologies

Fig. 1 shows a representative result of the PSAT degradation versus stress time for a population of G28 V3 devices under DC-ALT conditions at a typical accelerated junction temperature. The result shows that PSAT degrades over time in a well-behaved fashion with no abrupt or large changes. Empirically, the time dependence is observed to degrade as approximately sqrt(time), although the number of down points limits the ability to determine the functional form with a great deal of statistical confidence. The individual device lifetimes were determined by fitting the degradation to a sqrt(time) model and either interpolating or extrapolating to −1 dB. Fig. 1 shows that even after nearly 5000 h of stress at a highly accelerated condition, most devices still did not reach the −1 dB failure criterion. Therefore, the lifetimes of many of the devices had to be determined by extrapolation of a sqrt(time) fit. The degradation rate was found to be accelerated with junction temperature. This result is typical for temperatures across the ALT temperature range tested and is similar to results obtained for G28 V4 and G40 V4. These results are consistent with a common wear-out mechanism for the G28 V3, G28 V4, and G40 V4 technologies.

The PSAT degradation results are qualitatively consistent with a wear-out mechanism that occurs gradually over time, for example, material diffusion. The results are not consistent with a wear-out mechanism that results in abrupt and large changes in the device performance, for example, as has been reported by other institutions in the literature for the piezo-electric cracking failure mechanism [6]. Previous Wolfspeed publications have shown by physical failure analysis that the wear-out mechanism is source-side ohmic contact inter-diffusion and associated on-resistance increase, that results in the PSAT degradation; and that no evidence of piezo-electric cracking was observed after 28 V and 40 V ALT [1,4]. The failure analysis showed that