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Realistic non-destructive testing of integrated circuit bond wiring using 3-D X-ray tomography, reverse engineering, and finite element analysis

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ABSTRACT

Within industries that manufacture and/or utilize semiconductor devices, integrated circuit (IC) bond wiring is tested for product assurance and counterfeit detection purposes through invasive and destructive probing. The examined unit is either partially damaged or fully destroyed during these tests and the uncertainties that existed prior to testing reappear when a new unit must replace the probed unit. Because packaged circuits serve such diverse roles in countless critical systems across many applications, there is a strong need for robust, quick, and non-destructive testing. As of now, methods to non-destructively test these components involve either simplified geometric modeling and finite element analyses, which make concessions to accuracy, or include more accurate forms of geometric acquisition but remain untested, unverified, and computationally expensive. The goals of this study are to test the validity of micro-CT as a tool to import accurate bond wire geometries to single- and multi-physical finite element testing and to produce a practical methodology for the image acquisition, processing, and simulation of integrated circuit bond wires with a focus on practicality and industrial applicability. A reverse engineering technique is examined as a valid simplification to the geometries retrieved from micro-CT. The reverse engineered geometry from micro-CT is then tested within a finite element simulation with the loading data gathered from a traditional destructive bond wire pull-test to examine its similarity. The results show that the proposed methodology can closely mirror the destructive test by highlighting the correct location of probable failure with the corresponding stress values in excess of the material's strength limits. In addition, the methodology reduces the finite element computational expense by a factor of four and produces a CAD editable model for geometric alteration or other finite element testing environments; similar to the files created by part manufacturers prior to production. The differences being that the model can include production process-related variations and can be utilized by an end-user seeking validation for a given application. The broader implications of this methodology include its application to iterative product design and extension to multi-physical, dynamic, and/or inordinately expensive testing conditions.

1. Introduction

Bond wires are one of the primary vehicles for die to lead interconnection in packaged semiconductor devices. Some experts estimate that they account for roughly 95% of circulated device interconnections [1–6]. The quality of such interconnects largely affects the performance of the device and therefore it is essential for the manufacturers and industrial users to perform quality testing on the wires [7]. In addition to quality control, the proliferation of counterfeit electronics thrusted bond wire testing to an essential role in reliability and authentication testing. The specifics of these tests have been considered in published standards such as MIL STD 883, particularly the Method-2000 and Procedure-5000 series. Such tests can either be naturally destructive or non-destructive, but the majority require partial or full molding compound removal to access the internal attributes of the device. More modern standards like SAE AS6171, which is formatted for detecting counterfeit microelectronics, leverage some minimally invasive techniques such as X-ray computed tomography, in the case of SAE AS6171/5.

The destructive nature of decapping has many drawbacks, revealing a need for non-destructive methods. There are several notable advantages to the non-destructive evaluation of bond wires in integrated circuits using numerical simulation. To name a few [8]:

1. Reusability and assurance of the tested circuit are preserved during the test
2. Simultaneous testing of multiple components under different conditions is realized

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3. Complete control over tested bond wires with fine pitch/shared leads
4. Simulation offers significantly faster testing in long duration dynamic tests (i.e. fatigue, creep, etc.)
5. Ability to create extremely unique test environments that could be prohibitively expensive to recreate
6. Avoid unexpected effects on internal components during package removal processes (i.e. chemical bath, laser ablation, etc.)

Finite element testing of integrated circuit bond wiring has been attempted in the past but at some expense to accuracy [8–12]. The impact of variations in geometric modeling has been documented in the past yielding different simulation outcomes [13]. It was only until very recently that more robust and accurate approaches to incorporating realistic geometries have been proposed for FEA. To summarize the proposed technique for typical bond wire-pull or bond wire-shear tests, micro-CT is used to attain the actual geometry of the integrated circuit's bond wires. Then, through image processing and segmentation, the geometries can be directly imported to a simulation software for mechanical testing [7].

This new technique has opened the door for many possibilities. However, more development is needed before it can be considered for deployment in an industrial setting as an acceptable replacement for traditional destructive tests. First, the results of such an analysis have never been tested against the physical destructive bond wire tests that serve as the industry standard. The validity of this technique hinges on its ability to closely match the existing method of testing. Though it can be expected to yield relatively different results, given the destructive nature of the traditional testing method and the approximate numerical methods used.

In addition to verification of this technique's accuracy, to be deployed in an industrial setting, it needs to be practical. Some practical limitations of this type of analysis include the computational requirements and the need to prepare the model for FEA. It's an indisputable fact that a powerful CPU and GPU are needed for 3-D reconstruction. And it is known that the resulting segmented mesh for an arbitrary integrated circuit is quite large, often tens to hundreds of megabytes in size [9]. With simulation processes pushing the file size to roughly 10–100 times its original dimension, there is a debilitating bottleneck around the computation of high-resolution models. As mentioned before, the model preparation stage is an integral part of the simulation. Typically, FEA software packages are not designed for CAD modeling/repairing and lack the necessary tools. For a successful simulation, it is necessary to remove extraneous details from the tomography and to partition the model to define appropriate boundary conditions and loads.

These limitations leave the door open to more creative forms of FEM, like reverse engineering. The time spent computing these models, with a subject-matter expert (SME) present to correct any issues, correlates to a higher cost. To minimize these losses, a simple and thorough guideline is presented which can be expanded to any type of bond wire, cutting down the time required to set up the simulation and handle unexpected errors.

The final objective is to expand this testing method to the realm of multiphysics. As part of industrial reliability and quality assurance testing, integrated circuits are often subjected to thermo-mechanical testing (i.e. thermal cycling) [14]. Existing standards like JEDEC (JESD22-A104,-A106) and MIL STD 883 (Methods 1010, 1011, and 1012) detail the specifics for thermal and thermo-mechanical testing. In JESD22-A106 and Method 1011, a part is rapidly and harshly subjected to a number of cyclical thermal loads within a specialized thermal shock chamber. Then, visual and electrical examinations are performed at intervals to surmise if a failure has occurred via a bond interconnect or on the die face. This examination is highly sensitive to temperature values, peak temperature dwell times, and temperature settling time, all executed by an expensive and heavily taxed machine. By using FEA similar to those conducted in [10,15], or for the aforementioned Methods, then the scope of this technique becomes much more robust. The need for these specialized instruments begins to fade as do their limitations.

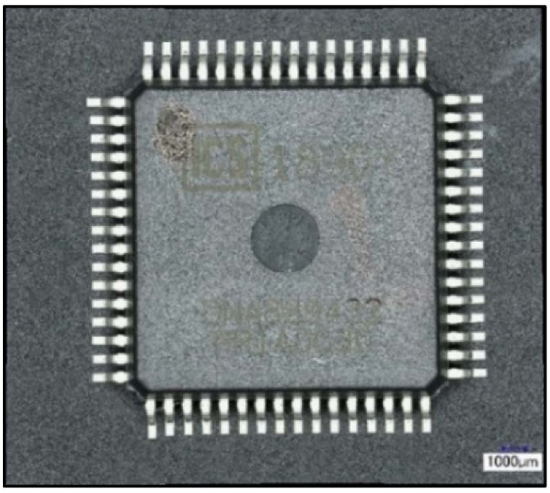

Fig. 1. Vertically stitched composite image of IC taken with Keyence VHX-2000 Digital Microscope (Itasca, IL).

2. Methodology

The integrated circuit that was selected for this study is pictured in Fig. 1. It is a QFP, single-die architecture part from Retail Alliance Limited (RAL) manufactured in Hong Kong (Part No.:A-4.0000-15). It is also shown in Section 3.1 through an SEM-EDS analysis, that the bond wires were Au and 30 µm in diameter. Also, the molding compound was determined to be a Si-based plastic and the lead frame, Sn-based. This model was selected randomly in hopes that this testing method would be indiscriminating.

2.1. Image acquisition

The circuit's tomography data was acquired with a Zeiss 510 Versa (Pleasanton, CA). It has a maximum resolution of roughly 700 nm and a maximum energy of 160 kV. The tomography parameters are listed in Table 1. Certain steps were taken to optimize the tomography that are outlined in other publications [16–17]. The primary goal was to attain the highest level of resolution without compromising the field of view, an acceptable signal to noise ratio, or scan time. The field of view is presented in Fig. 2.

The coupled nature of pixel size and field of view is a physical limitation of the detector but can still be addressed. Many micro-CT systems possess the ability to stitch projections vertically and some even laterally, similar to a wide-field optical objective. Introducing this powerful imaging tool allows an industrial investigator to produce a 3-D volume at high resolution for any region of interest. But ultimately, the selection of field of view/pixel size will be limited by the wire length and diameter. It cannot be too small such that at least one wire

Table 1
Tomography parameters.

Pixel Length (µm)	3.74
Field of View (µm × µm)	3825 × 3825
Objective	0.4×
Energy (kV)/Power (W)	150/10
Time of Tomography (hours)	3.5
Number of Projections	1600
Rotated Angle (°)	180