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Radiation Hardened by Design Latches — A Review and SEU Fault Simulations

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ABSTRACT

There are many Radiation Hardened by Design (RHBD) architectures presented in the literature to mitigate Single Event Upset (SEU) in a storage element, a latch. Nevertheless, the design of a SEU hardened latch is being continuously improved with respect to reliability, performance, power consumption and area overhead. SEU mitigating techniques by design focus on reducing criticality of sensitive nodes in a latch. Sensitive node(s) in a latch could be an active and/or a high impedance node(s). In this paper, we have classified previously presented SEU hardened by design latch architectures and reviewed SEU mechanisms in selected RHBD latch architectures on Complementary Metal Oxide Semiconductor (CMOS) technology models. Simulation studies using latest fault simulation model have been carried out. Simulation results have revealed some interesting observations described in this paper. Our findings, based on analyses, will provide valuable design inputs for futuristic RHBD latches with advanced technology nodes.

1. Introduction

CMOS logic and memory devices used in digital systems of a spacecraft can get perturbed, if an ionizing radiation particle (ion, electron or proton) strikes at their sensitive nodes. Perturbation, a bit flip, is a soft error in logic or memory devices and known as single event upset (SEU) [1]. The rate at which number of upsets per unit time occur in a storage element is known as soft error rate (SER). SER is an important metric in the availability estimation of a spacecraft [2]. Therefore, it is necessary to mitigate the SER to an acceptable level [3]. SEU tolerance capability of a RHBD latch varies with circuit topology, fabrication technology, supply voltage, temperature, transistor geometry and load capacitance. At device level, there are two techniques to mitigate the SER viz. Radiation Hardened by Process (RHBP) and Radiation Hardened by Design (RHBD). The RHBP techniques involve modification of geometrical parameters of CMOS transistors during development of the device fabrication process. The techniques such as resistive hardening, Silicon on Insulator (SOI), well-contacts, guard bands, or guard rings can reduce SER but they are technology dependent [4–7]. On the other hand, the RHBD techniques focus to reduce the criticality of sensitive nodes through incorporation of redundancies and filters during the design of a storage cell architecture. The RHBD techniques usually introduce an overhead on CMOS Integrated Circuit (IC) in terms of its area, power consumption, timing and costs, but they are independent of technology advancement as they do not need alteration in IC fabrication process or use of specific materials. This feature of the RHBD techniques attracted researchers to develop many variants of circuit level Multiple Modular Redundancy (MMR) architectures [4,5], [8–32] to prevent or manage a single node and multiple nodes SEU in last three decades. In this paper, we have reviewed and classified some of the architectures presented in the last three decades based on their SEU tolerant technique in three broad categories viz. node interlocking latch architectures (NIA) [8–10] [12,15,24,25,27,31,32], feedback blocking latch architectures (FBA) [16,18,20,22,26,28,29] and C-element or hysteresis based latch architectures (CHA) [11,13,14,17,19,21,23,30].

We have evaluated few RHBD latch architectures of each category on multiple technology nodes viz. 180 nm, 90 nm, 65 nm, 45 nm, 32 nm and 22 nm. As reported in literature [33,34], usage of double exponential current model (traditional method for robustness investigation of a RHBD latch [35,36]) is not sufficiently accurate for deep submicron CMOS technologies. In view of this we have used both double exponential (DE) and the latest dual double exponential (DDE) current [33] models to evaluate SEU tolerance capability of RHBD latches.

The rest of this paper is organized as follows: an overview of the SEU phenomenon in basic latch and basis of categorization of RHBD latches briefly described in Section 2. Transient fault simulation

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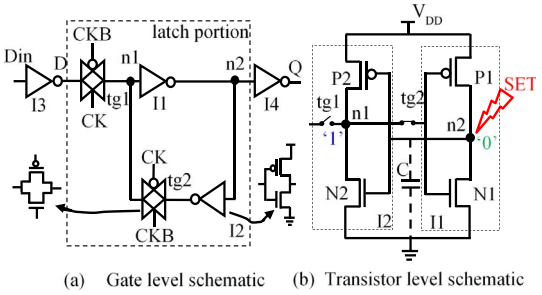

(a) Gate level schematic (b) Transistor level schematic

Fig. 1. Basic latch (un-hardened latch).

methodologies and mechanisms are discussed in Section 3. SEU in terms of critical charge and simulation results are summarized in Section 4. Finally, Section 5 presents the conclusions of this paper.

2. Background

2.1. SEU mechanism in basic latch

The basic latch (BL) [14,37] shown in Fig. 1 (gate schematic in Fig. 1(a) and its equivalent transistor circuit in Fig. 1(b)) is the fundamental element of digital sequential logic and memory circuits. During write mode clock signals CK and CKB go high and low which enable transmission gate tg1 and disable tg2. During hold mode tg1 get disabled and tg2 get enabled and nodes n1 and n2 store valid logic values. The stored logic values at the nodes n1 and n2 are complement of each other as shown in Fig. 1(b). If the logic values at these nodes get inverted spuriously then the latch is said to be upset. It happens in space-borne digital systems when a charged particle sourced from the sun or other galaxies strikes at the node n1 or n2 or D. These nodes are critical as a charged particle impact perturbed the latch till next write operation.

Drain-bulk junction of off transistors connected to a node in a latch is sensitive to radiation effect [37]. With a charged particle strike at the drain of off transistor of a latch, a voltage transient gets generated which is termed as a single event transient (SET). Transient voltage level depends on load capacitance C, supply voltage and drain area of off transistor. When charge collection at the affected node, n2 in Fig. 1(b), reaches a critical value (Q_{crit}), the generated voltage ($V = Q_{crit}/C$) equals to the threshold voltage (V_{th}) of inverter I2; at the node n1, output voltage of inverter I2 begins to fall as a consequence of transient fault (TF) at node n2 [38]. If voltage fall at the node n1 crosses the threshold voltage of inverter I1 then node n2 does not come back to its pre-strike logic state and the latch remains in this condition till the next write operation. This unwarranted state inversion phenomenon in the storage element during latch phase is known as upset and it is an effect of a single ion hit on a sensitive/critical node; hence, termed as single event upset (SEU) [39]. Similar phenomenon happens when a charged particle hits at node n1.

In the case of input node, propagation of a fault through nominally off transmission gate, tg1, depends on supply voltage of the latch circuit [40]. Nevertheless, the input node of a latch is robust than the internal nodes.

To prevent SEU, many researchers proposed RHBD techniques/latches.

2.2. Categorization of latch architectures

We have categorized the RHBD latch architectures in three broad categories viz., Node Interlocking Architectures (NIA), Feedback Blocking Architectures (FBA) and C-element or hysteresis based architectures (CHA) based on their SEU tolerance techniques. Few representative RHBD latches from each class and their associated intricacies are highlighted in TABLE 1. Basic elements used in latch architectures are: transmission gate, pass transistor, two inputs separated gate inverter, regular static inverter and C-elements. In most of the RHBD latches, use of symmetrical or asymmetrical C-elements [41] are found to be common. C-element isolates propagation of a fault from its input to the output when SET strikes at an input node, reduces dynamic power consumption and converges multiple nodes logic level into a single output. The configuration and control of the basic elements in a RHBD latch design in a systematic fashion defines the SEU tolerance technique used in that particular architecture.

Table 1
Categorization of latches.

Category	Cell type	Critical nodes	'Z' nodes	No. of transistors*	Additional requirement
NIA	BL [14]	3	0	8	Nil
	TILL [25]	2	0	22	Nil
	DICE [10]	2	0	12	Input buffer sizing
FBA	FBT [16]	5	2	8	Refresh circuit
	DICE-FBT [29]	2	4	16	Input buffer sizing and refresh circuit
	RHD11 [28]	3	2	11	Input buffer sizing, access transistor sizing and refresh circuit
CHA	CE [11]	1	0	10	Input buffer sizing
	mCE [24]	1	0	18	Input buffer sizing
	AD1V2 [30]	1	0	22	Input buffer sizing

Notes: 'Z' high impedance nodes, *excluding input and output buffers.

2.2.1. Node Interlocking Architectures (NIA)

Internal nodes of these types of latch architectures [8–10], [12,15,24,25,27,31,32] are always active during hold mode i.e., a node of an NIA either switched to supply or ground; hence, they do not need refresh circuit. Perturbed node(s) is repaired by copying content from healthy redundant node during a charged particle strike. Sizing of write buffer is required to avoid an electrical conflict between the input and internal nodes during write operation.

2.2.2. Feedback Blocking Architectures (FBA)

These types of latch architectures [16,18,20,22,26,28,29] use static and dynamic CMOS logic. Transient fault propagation from output to input and vice versa is prevented through normally off feedback transistors. Few of the internal nodes of these types of latch architectures are always in high-impedance state during latch phase and need a refresh circuit. This type of architectures does not possess electrical conflict except DICE (Dual Interlocked Storage Cell) based architecture.

2.2.3. C-element or hysteresis based architectures (CHA)

These types of latch architectures [11,13,14,17,19,21,23,30] consist of active and/or high impedance internal nodes during latch phase. In few latches, the output node takes high impedance state when any one of its input node gets upset due to a charged particle strike. SET pulse is filtered out at the input so as its propagation to output is blocked in this type of architectures. Hysteresis based architectures are designed in such way that propagation delay of the circuit is greater than the anticipated transient pulse duration. Sizing of write buffer may be needed to avoid electrical conflict between the nodes and improve performance.

3. Simulation studies

Primary aim of our simulation studies was to identify critical nodes of a RHBD latch circuit published in the literature and understand upset