Microelectronics Reliability 83 (2018) 157–161

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

# Scalability comparison between raised- and embedded-SiGe source/drain structures for $Si_{0.55}Ge_{0.45}$ implant free quantum well pFET

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ARTICLE INFO

*Keywords:*
SiGe channel
Raised source/drain
Embedded SiGe stressor
Epitaxy
Quantum well

ABSTRACT

In this work, we have studied gate length ($L_{gate}$) scalability of $Si_{0.55}Ge_{0.45}$ Implant Free Quantum Well (IFQW) pFET with raised and embedded $Si_{0.75}Ge_{0.25}$ source/drain structures. Although embedded SiGe device shows higher $I_{dsat}$ which can be attributed to thinner $T_{inv}$ (more scavenging of High-k interfacial layer), raised SiGe device has better short channel control than embedded SiGe device thanks to shallower junction depth. Raised SiGe device can scale down $L_{gate}$ by 4 nm compared to embedded SiGe device while maintaining identical $I_{off}$. This results in superior intrinsic delay in raised SiGe device.

## 1. Introduction

CMOS device scaling has been continuing for past several decades to achieve higher performance and lower power consumption with even lower cost. As traditional bulk planar device structure reached its physical limitation, FinFET or multi gate FET has been introduced in the industry several years ago either on bulk substrate [1,2] or on SOI substrate [3]. FinFET has provided higher transistor performance and lower off-state leakage concurrently thanks to its superior electrostatic control [1].

Despite this superior performance, FinFET technology has several challenges such as process complexity and process variability [4].

There have been some proposals for alternative device architectures to achieve further device scaling but with relatively smaller additional complexity. One is Fully Depleted SOI (FD-SOI) architecture where SOI channel is aggressively thinned down to suppress short channel effect [5–7]. FD-SOI is a planar structure, therefore additional process complexity compared to bulk planar devices is relatively smaller than FinFET.

Another candidate is the implant free quantum well (IFQW) structure which has been proposed in ref. 8. This IFQW FET is bulk planar device and has lower band gap material like SiGe as a channel on Si substrate [8–12]. In the SiGe IFQW pFET case, holes are confined in SiGe layer due to valence band offset between SiGe and Si substrate and it was demonstrated to reduce S/D leakage in Si substrate and to improve short channel effect [13].

Previous reports studied intensively channel strain applied from two kinds of source/drain (S/D) structures on SiGe IFQW devices, namely raised SiGe S/D and embedded SiGe S/D [11,12,14]. It was found that embedded SiGe S/D and raised SiGe S/D provides similar amount of strain in the channel with optimized process, hence similar drive current was observed between those two kinds of S/D structures.

In this work, we investigated those two kinds of S/D structures from gate length scaling point of view and assessed AC performance.

## 2. Experiments

Device fabrication flow is shown in Fig. 1. In this work, we fabricated two kinds of devices. One is “rSiGe” device which only has raised SiGe S/D (Fig. 2a). The other is “eSiGe” device which has both raised SiGe and embedded SiGe S/D (Fig. 2b).

After shallow trench isolation (STI) is formed, well and channel doping and annealing are done. Then, non-doped $Si_{0.55}Ge_{0.45}$ channel is epitaxially grown on Si substrate (4 nm). Secondary ion mass spectroscopy (SIMS) analysis was done on the $Si_{0.55}Ge_{0.45}$/Si structure, and the result is shown in ref. 16. As shown in ref. 16, as-grown SiGe layer has approximately 45% peak Ge concentration. $Si_{0.55}Ge_{0.45}$ layer is compressively strained (biaxial) as lattice constant of $Si_{0.55}Ge_{0.45}$ is larger than that of Si [15]. Si-cap layer is successively deposited on top of $Si_{0.55}Ge_{0.45}$ layer to keep high quality interface with high-k gate stack. As valence band maximum is energetically higher for $Si_{0.55}Ge_{0.45}$ than Si [17], holes are confined in the $Si_{0.55}Ge_{0.45}$ QW layer. After interfacial

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https://doi.org/10.1016/j.microrel.2018.03.006
Received 30 October 2017; Received in revised form 24 January 2018; Accepted 4 March 2018
Available online 20 March 2018

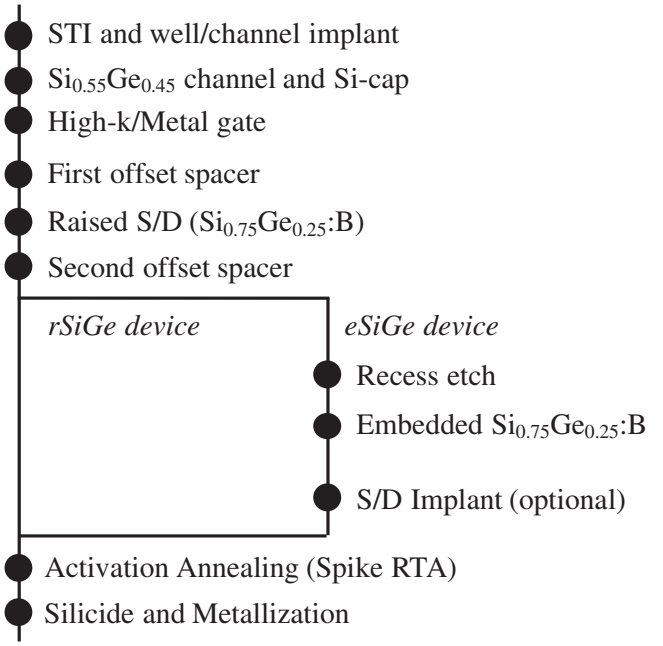


**Fig. 1.** Fabrication flow of SiGe IFQW device with raised SiGe and embedded SiGe source/drain.

layer growth (chemical oxide), $HfO_2$ high-k dielectric (1.8 nm) and PVD-TiN (2 nm) metal gate electrode are deposited and gate etch follows. First offset spacer (6 nm) is formed and *in-situ* boron doped $Si_{0.75}Ge_{0.25}$ is epitaxially grown as raised S/D. Thickness of this raised SiGe layer is 50 nm for rSiGe device and 30 nm for eSiGe device. Then second offset spacer is formed. rSiGe device and eSiGe device have common process flow up to this second spacer formation step except for raised $Si_{0.75}Ge_{0.25}$ thickness. For eSiGe device, raised $Si_{0.75}Ge_{0.25}$ and Si substrate is recessed and *in-situ* Boron doped $Si_{0.75}Ge_{0.25}$ is again grown as embedded stressor. Recess depth (with respect to original SiGe channel surface) is 60 nm and over fill is 30 nm. Additional S/D implant is done as optional step (boron 3 keV, $3 \times 10^{15}$ cm$^{-2}$) to see how device performance and short channel effect are modulated. rSiGe device skips recess etch and embedded $Si_{0.75}Ge_{0.25}$ growth. Then both devices receive spike rapid thermal anneal (spike RTA, 950 °C) to create a certain amount of overlap to channel with diffused boron from raised SiGe S/D. After spike RTA, Ni silicidation, contacts formation and metallization process follow.

Both raised and embedded $Si_{0.75}Ge_{0.25}$ films have boron concentration of about $1 \times 10^{20}$ cm$^{-3}$.

Cross-sectional transmission electron microscopy (XTEM) images of rSiGe and eSiGe device are shown in Fig. 2(a) and (b) respectively. Note that raised SiGe is still left next to first offset spacer in eSiGe device. The epitaxial $Si_{1-x}Ge_x$ and Si layers were grown in an ASM Epsilon™3200.

## 3. Results and discussions

Fig. 3 shows the $I_{dsat}$-$I_{off\_d}$ curve for rSiGe and eSiGe (w/ and w/o S/D implant) device ($V_{dd} = -1$ V). eSiGe device has about 8% higher $I_{dsat}$ than rSiGe device at fixed $I_{off\_d}$ of 100 nA/μm (1040 μA/μm for eSiGe device without S/D implant, 1036 μA/μm for eSiGe device with S/D implant, 965 μA/μm for rSiGe device). Comparable drive current between two eSiGe devices (with and without S/D implant) is likely because lower external resistance with S/D implant is offset by higher channel resistance due to longer gate length at target $I_{off\_d}$ (100 nA/μm). Some outliers seen on rSiGe device are due to high junction leakage (S/D junction can be located very close to or within $Si_{0.55}Ge_{0.45}$ channel layer, therefore any crystal defect can cause very high leakage. This needs to be solved by less defective epitaxial process).

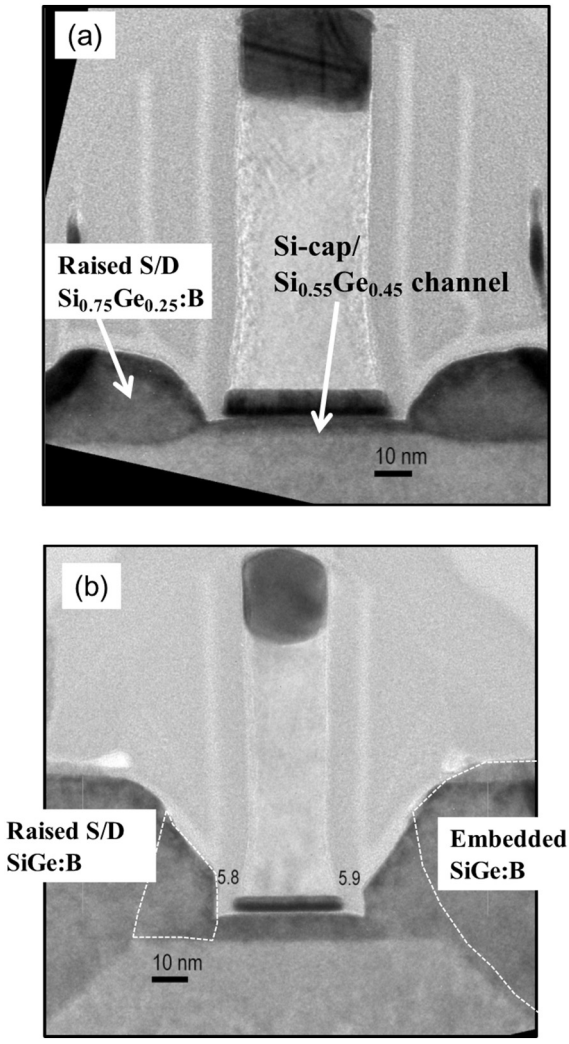


**Fig. 2.** XTEM images of fabricated $Si_{0.55}Ge_{0.45}$ IFQW device with (a) raised SiGe S/D and (b) embedded SiGe S/D.

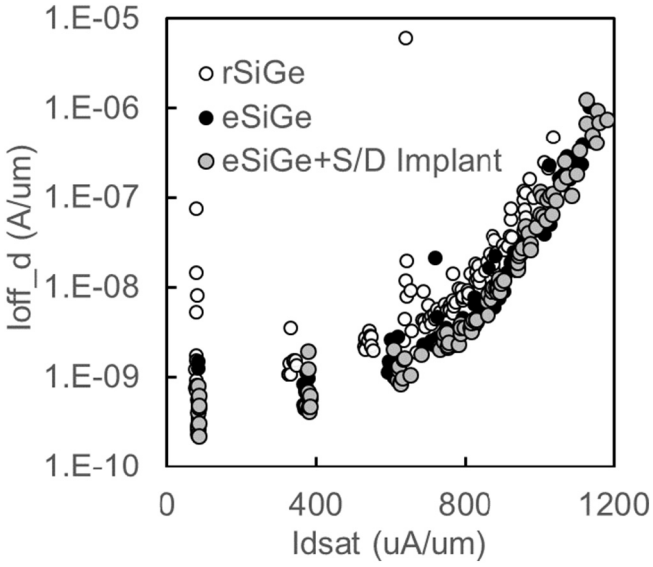


**Fig. 3.** $I_{dsat}$-$I_{off\_d}$ for rSiGe and eSiGe devices (w/ and w/o S/D implant).