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Dual-resonance concurrent oscillator

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ABSTRACT

This paper studies a new dual-band CMOS class-C voltage-controlled oscillator (VCO). The oscillator consists of a dual-resonance LC resonator in shunt with two pairs of capacitive cross-coupled nMOSFETs. The proposed oscillator has been implemented with the TSMC 0.18 μm CMOS technology, and it shows a frequency tuning range with two frequency bands and a small tuning hysteresis is measured. The oscillator can generate differential signals at 2.4 GHz and 6.9 GHz and it also can generate concurrent frequency oscillation while the circuit is biased around the bias with frequency tuning hysteresis. With the supply voltage of $V_{DD} = 1.1$ V, the VCO-core current and power consumption of the oscillator are 2.90 mA and 3.19 mW, respectively. The die area of the class-C oscillator is 0.9×0.97 mm^2. Overvoltage stress is applied to the oscillator, measurement indicates the concurrent oscillation is sensitive to overvoltage stress.

1. Introduction

The evolution of wireless communications attracts an interest toward the development of multi-band and multi-standard systems with minimal hardware implementations. Multi-band CMOS voltage-controlled oscillators (VCOs) can be used in multi-standard consumer wireless transceivers. In conjunction with mixers they are used primarily for frequency translation. Concurrent oscillation is a phenomenon that a circuit can output two harmonically unrelated frequency signals simultaneously. Concurrent oscillators are a type of multi-band oscillators and can be implemented in concurrent dual-band receiver [1], phase locked loop and multifunctional transceiver [2] and they [3,4,5] have been implemented with two cross-coupled n-core oscillators coupled via magnetic field through the use of coupled inductors. Concurrent oscillators [6] also can be implemented with cross-coupled n-core and p-core oscillators. The reported Colpitts [7,8] Hartley concurrent used a fourth-order LC tank.

The topic of concurrent oscillators is not attractive as dual-band oscillators, as no significant industry application is used today. However, often an important application evolves as useful information accumulates. This paper studies a dual-band oscillator, which can serve as a concurrent oscillator designed in CMOS. At the supply voltage 1.1 V, by tuning the control voltage, the CMOS dual-resonance VCO can generate a low-band signal at 2.4 GHz and a high-band signal at 6.5 GHz and concurrent oscillations at 2.4 GHz and at 6.5 GHz. A frequency tuning hysteresis is found in the studied VCO and is not found in the previous concurrent oscillators [1–8]. Over-voltage stress is applied to the VCO to see the hot-carrier effect on the concurrent oscillation, measurement indicates sensitive variation to overvoltage stress.

2. Circuit design

Fig. 1 shows the schematic of the designed CMOS VCO with two sub-oscillators. The first oscillator uses an LC-tank resonator and a cross-coupled pair (M_{12}, M_{13}) to generate negative resistance to compensate for the resistive LC-tank loss. MIM capacitors (C_3, C_4) are dc blocking capacitors. Resistors (R_3, R_4) are used for dc biasing. The LC resonator consists of a center-tapped inductor L_1, inductors (L_2, L_3), and accumulation-mode varactors (C_{v1}, C_{v2}), and parasitic capacitor C_p across the drains of the switching pair. The varactor bias V_T is the varactor control voltage and is used to enable/disable the inverter and the MOSFETs (M_7, M_8) form an inverter. The C_6, M_9, (M_{10}, M_{11}) form the first bias circuit to control the V_{Gd} [9,10]. During the start-up transient, C_6 is charged to high voltage through M_9, the gate bias of M_{12} is high. After the start-up oscillation, (M_{10}, M_{11}) are switched on periodically. This discharges the capacitor C_6 and the gate bias V_{Gd} of M_{12} decreases. The nMOSFETs (M_{14}, M_{15}) are output buffers with drain bias V_{buffer}. The bias V_{DD} is the supply voltage. The bias V_{CH}/V_{CL} is the supply voltage for bias circuits.

The second oscillator uses a capacitive cross-coupled pair composed of (M_4, M_5), MIM capacitors (C_1, C_2) and resistors (R_1, R_2). The C_5, M_1, (M_2, M_3) form the second bias circuit to control the gate voltage V_{Gu}. The dynamic bias circuit is used to improve the dc-RF conversion efficiency so that low power oscillator can be designed. M_6 is the tail transistor. The above components in conjunction with inductor L_1 and

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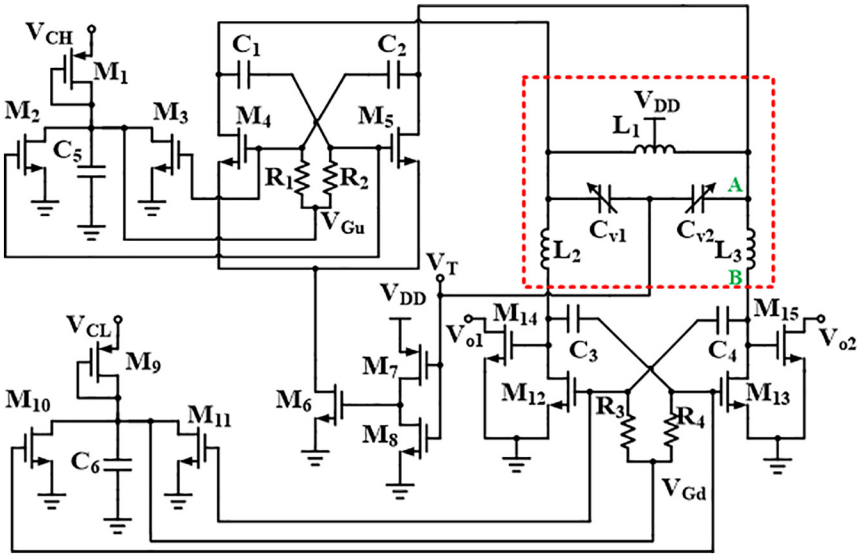

Fig. 1. Schematic of the proposed DB concurrent VCO.

varactors (C_{v1}, C_{v2}) form an oscillator. The above two oscillators share the same resonator. For a single-resonance oscillator, the oscillation frequency satisfies the Barkhausen criteria. For a dual-resonance oscillator, if the two oscillation frequencies satisfy the Barkhausen criteria, the oscillator outputs two frequency signals otherwise it outputs only one fundamental signal and its harmonics.

Fig. 2(a) and (b) show the simulated voltage transients. At $V_T = 0$ V, M_6 is on, the second oscillator is turned on, the simulated oscillation frequency is 2.5 GHz; the second oscillator dominates, the voltages at node A and B are in-phase. The resonant frequency is determined by inductor L_1 and varactors (C_{v1}, C_{v2}). Because the capacitance of (C_{v1}, C_{v2}) is large the oscillation frequency is small. At high-level V_T, M_6 is off, the second oscillator is turned off. At $V_T = 2$ V, the simulated oscillation frequency is 7.45 GHz. The resonant frequency is determined by inductors (L_2, L_3), and parasitic capacitor across the drains of (M_{12}, M_{13}), and varactors (C_{v1}, C_{v2}) are considered as short circuit because of large varactor capacitance. At $V_T = 2$ V, the first oscillator dominates, the voltages at node A and B are out-of-phase due to the standing wave nature and in practical (C_{v1}, C_{v2}) are not completely considered as short circuit. Fig. 3 shows the simulated tuning range. As V_{DD} increases, V_T (at frequency band-transition) increases because the inverter requires higher V_T to switch from high- to low-level. Fig. 4(a)/(b) is an expanded view of Fig. 3. As V_C increases, the gate voltages V_{Gd} and V_{Gu} increase, and the VCO voltage swing increases and the power consumption increases.

Fig. 5(a) shows the simulated voltage transients. The voltage has no visual steady output because of concurrent oscillation and mixing products of concurrent oscillation signals. The Discrete Fourier Transform (DFT) output in Fig. 5(b) shows two tones at 7.05 GHz and 2.55 GHz. At $V_T = 0.5366$ V the two sub-oscillators are on, therefore the VCO provides the primary signals at two oscillation frequencies.

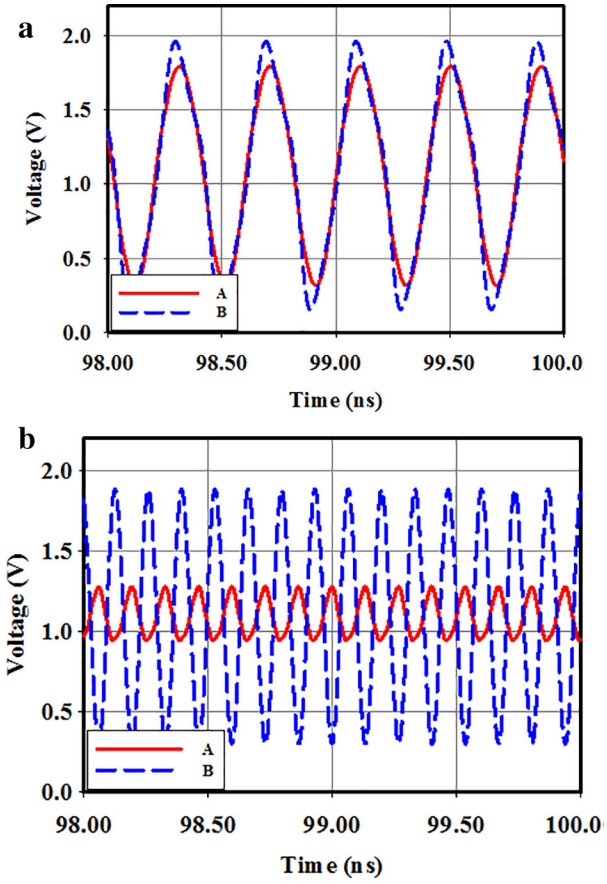

Fig. 2. Simulated voltages at nodes A, B in Fig. 1. (a) $V_T = 0$ V, (b) $V_T = 2$ V. $V_C = V_{CH} = V_{CL} = 1.25$ V, $V_{DD} = 1.1$ V. $V_{buffer} = 0.7$ V.

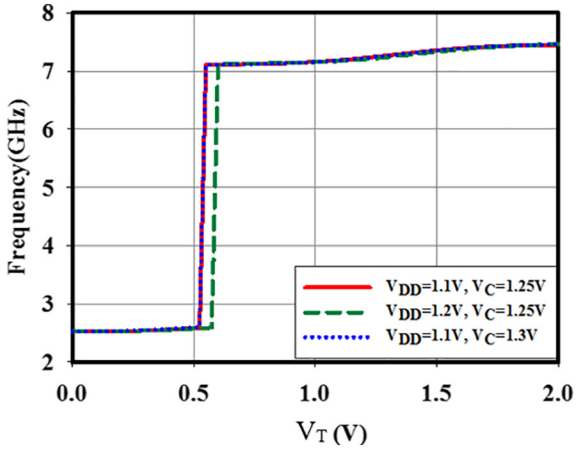

Fig. 3. Simulated tuning range versus V_T. $V_C = V_{CH} = V_{CL}$, $V_{buffer} = 0.7$ V.

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