Microelectronics Reliability xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Investigation and application of vertical NPN devices for RF ESD protection in BiCMOS technology

Guo-Lun Huang, Wei-Hao Fu, Chun-Yu Lin *

Department of Electrical Engineering, National Taiwan Normal University

ARTICLE INFO

Article history:
Received 14 January 2017
Received in revised form 11 May 2017
Accepted 27 June 2017
Available online xxxx

Keywords:
BiCMOS technology
Electrostatic discharge (ESD)
Low-noise amplifier (LNA)
Radio-frequency (RF)
Vertical NPN (VNPN)

ABSTRACT

BiCMOS technologies have been used to implement the radio-frequency (RF) integrated circuits (ICs) due to the advantages of low noise, low power consumption, high drive, and high speed. The electrostatic discharge (ESD) is one of the important reliability issues of IC. When the ESD events happen, the ESD protection devices must be turned on immediately to protect the ICs, including the RF ICs in BiCMOS technologies. In this work, the vertical NPN (VNPN) devices in 0.18 μm silicon-germanium (SiGe) BiCMOS technology with base-emitter shorted and resistor trigger approaches are investigated. In component-level, using transmission-line-pulsing (TLP) and ESD simulator test the I—V characteristics and human-body-model (HBM) robustness of the VNPN devices, respectively. In system-level, using ESD gun tests the system-level ESD robustness. The ESD protection of VNPN devices are further applied to a 2.4 GHz low-noise amplifier (LNA). After attaching the VNPN devices to LNA, the RF characteristics are not degraded while the ESD robustness can be much improved.

1. Introduction

Since the development of integrated circuits (ICs), electrostatic discharge (ESD) is always an important reliability issue [1]. ESD may cause a large current (several amperes) in a short time (nanoseconds), and it often results in damages in IC products and increases defect rate. An electric charge through human-body and metallic tool flow into the IC and the system, leading to component-level and system-level ESD events [2]. Many papers have concerned about the ESD issues in CMOS technologies. Besides, the ESD issues in BiCMOS technologies should also be taken care. BiCMOS technologies have been used to implement the radio-frequency (RF) integrated circuits (ICs). Using SiGe BiCMOS technology leads to good performances, including low noise, low power consumption, high drive, and high speed [3], but the circuits still need to concern the ESD issues. If an ESD stress to the IC, it makes the IC lose its original characteristics, and this is irreversible. Thus, the ESD protection design must be equipped to the IC products. A general ESD protection window is shown in Fig. 1 [4], where the protection device should turn-on in the specified region defined by the supply voltage (V_{DD}) and the internal circuit breakdown voltage (V_{BD}). If the holding voltage (V_h) is lower than V_{DD}, there will be latch-up issues [5]; if the trigger voltage (V_{t1}) is higher than V_{BD}, the circuit cannot be protected from ESD damage [6]. The designers must make sure that the ESD protection device conforms to ESD protection window. Besides, the ESD protection device should not degrade the RF characteristics [7,8].

When ESD events happen, a low-noise amplifier (LNA), which is input terminal of RF transceiver [9], is the earliest to suffer ESD damage in the RF circuits. To improve the ESD robustness, adding effective on-chip ESD protection device is a good way to prevent IC from ESD damages. This paper presents the ESD protection of the vertical NPN (VNPN) devices with two approaches [10]. One of approaches is base-emitter shorted and the other one is resistor trigger with different resistance values. After investigating the performances of the VNPN devices, the VNPN devices are further applied to a 2.4 GHz LNA, that is used two-stage and cascode architecture –[11–14]. The characteristic of LNA is simulated with different sizes and approaches of VNPN devices in 0.18 μm SiGe BiCMOS process. In this paper, the design, measurement, and application of VNPN devices are discussed in Sections 2, 3, and 4, respectively.

2. Structure of vertical NPN devices

Fig. 2(a) and (b) show the VNPN devices with base-emitter shorted and resistor trigger, respectively. In the VNPN devices, currents flow from RF_{in} pad to V_{SS} through the two paths to protect internal circuits

* Corresponding author.
E-mail address: cy.lin@ieee.org (C.-Y. Lin).

http://dx.doi.org/10.1016/j.microrel.2017.06.068
0026-2714/

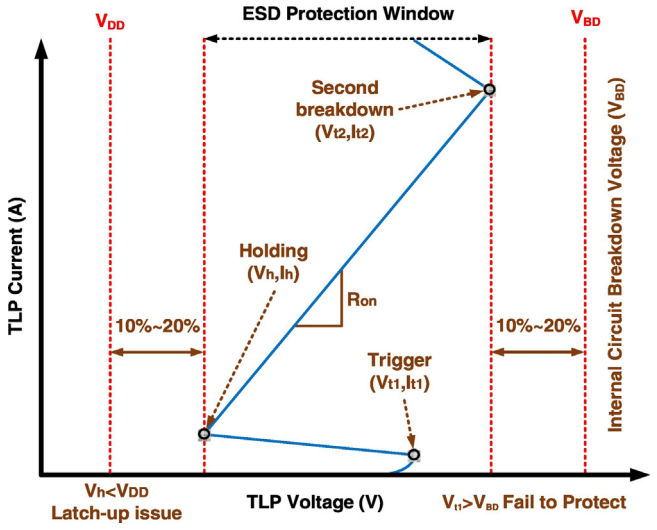

Fig. 1. ESD protection window.

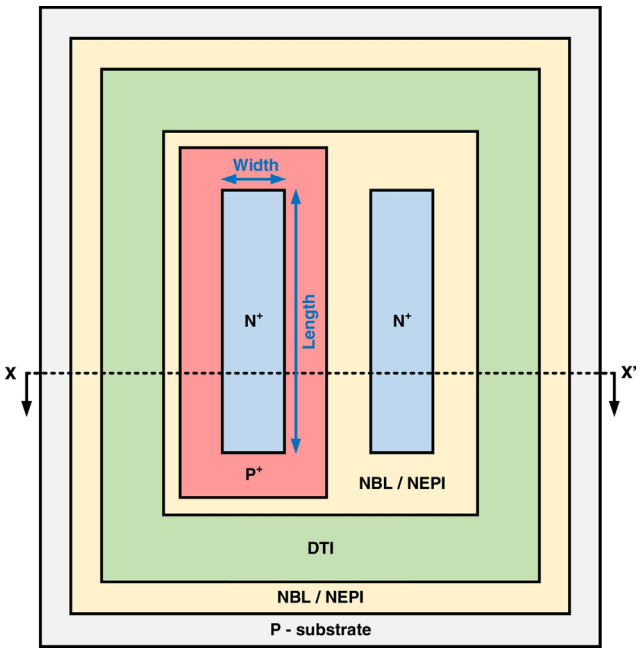

Fig. 3. The layout top view of VNPN device.

during ESD events: through ESD path I if the ESD is positive at RF_{in} pad, and through ESD path II if it is negative at RF_{in} pad. The layout top view of VNPN device is shown in Fig. 3. Along X-X′, it includes P-substrate, N^+ Buried Layer (NBL), N^+-EPI (NEPI), deep trench isolation (DTI), P^+, and N^+. The cross sectional view of VNPN devices with base-emitter shorted and resistor trigger are shown in Fig. 4(a) and (b), respectively. The ESD path I (N^+/NBL/NEPI/P^+/N^+) from RF_{in} pad to V_{SS} discharges ESD current during positive ESD event at RF_{in} pad, and the ESD path II (N^+/P^+/NBL/NEPI/N^+) from V_{SS} to RF_{in} pad discharges ESD current during negative ESD event at RF_{in} pad. In the base-emitter shorted way, base-emitter (P^+-N^+) are shorted, and base-collector forms P^+-N^+ junction just like a diode. However, base-emitter shorted approach which increase trigger voltage causing the VNPN device cannot quickly turn-on to protect internal circuit during positive ESD event at RF_{in} pad. In the resistor trigger way, the resistor (R_{tri}) reduces the trigger voltage, and the VNPN device with lower trigger voltage can turn-on faster to protect the internal circuit.

3. Verification of vertical NPN devices in component-level ESD and system-level ESD

The VNPN devices with base-emitter shorted and resistor trigger have been fabricated in BiCMOS technology. Table 1 shows the different sizes of VNPN devices, in which all the widths of test devices are 0.2 μm and the lengths include 60 μm, 180 μm, and 360 μm. The resistance values of R_{tri} in VNPN devices with resistor trigger include 100 kΩ and 500 kΩ.

A. Component-level ESD test

In component-level, using transmission-line-pulsing (TLP) system observes I—V characteristics of ESD devices [15,16]. Besides, using ESD simulator tests the human-body-model (HBM) ESD robustness [17,18], and the result is an important indicator of IC reliability.

The TLP I—V curves of VNPN devices during positive stresses at RF_{in} pad are shown in Figs. 5 and 6. In order to determine whether the ESD devices damaged or not, observing leakage current of devices is a way. When leakage current suddenly increases, it represents devices short; when leakage current suddenly decreases from large to small, it represents metal lines open. From the leakage current offset >30% to determine the VNPN devices burned, according to the measurement results, the failures are all because of devices short. The measurement results show that the VNPN devices with base-emitter shorted have higher

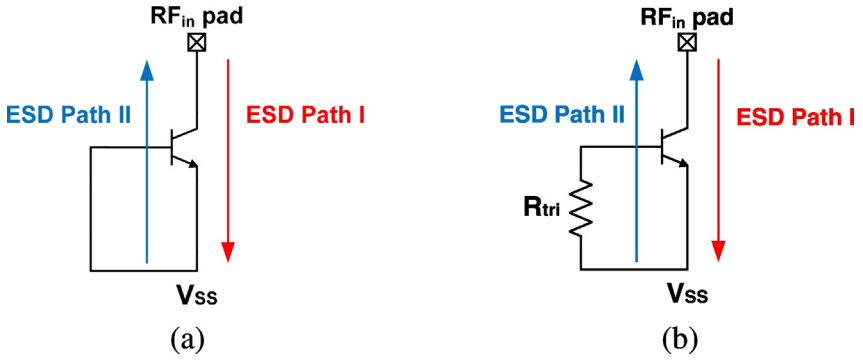

Fig. 2. The VNPN devices with (a) base-emitter shorted and (b) resistor trigger.

Please cite this article as: G.-L. Huang, et al., Investigation and application of vertical NPN devices for RF ESD protection in BiCMOS technology, Microelectronics Reliability (2016), http://dx.doi.org/10.1016/j.microrel.2017.06.068