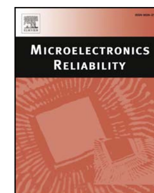
Microelectronics Reliability 82 (2018) 84–89

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Parameter driven monitoring for a flip-chip LED module under power cycling condition

J. Magnien[a,*], L. Mitterhuber[a], J. Rosc[a], F. Schrank[b], S. Hörth[c], M. Hutter[d], S. Defregger[a], E. Kraker[a]

[a] Materials Center Leoben Forschung GmbH (MCL), Roseggerstraße 12, A-8700 Leoben, Austria
[b] Tridonic Jennersdorf GmbH, Technologiepark 10, A-8380 Jennersdorf, Austria
[c] Häusermann GmbH, Zitternberg 100, A-3571 Gars am Kamp, Austria
[d] Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration, Gustav-Meyer-Allee 25, D-13355 Berlin, Germany

ARTICLE INFO

Keywords:
Monitoring model
Reliability model
Thermal resistance
Thermal impedance analysis
Flip-chip LED
Power cycling test
Solder fatigue

ABSTRACT

In this paper, a parameter driven monitoring model is introduced, in which a flip-chip LED module was investigated during a power cycling test. This approach was investigated to develop a monitoring model to describe thermally induced solder fatigue as root cause of flip-chip failure in a power cycling test. As monitoring parameter the thermal resistance of the LED module was used, which was determined by thermal impedance measurements of the whole LED module, as well as for each LED chip itself. Further analyses of the occurring temperature at the LED junction recorded of each chip during the power cycling test were used to generate a prediction model. The evaluation of the temperature change allowed to forecast the number of cycles until failure.

1. Introduction

Flip-chip mounting is one of the advanced interconnection techniques, which is used in the solid state lighting industry and it is becoming more popular, due to size and thereby cost reduction. Furthermore, the high light output with a very low energy consumption has attracted much interest in indoor lighting, automotive lighting and street lighting. In these fields of applications, the reliability of flip-chip LEDs plays an important role due to the exchange of LED devices can be cost-intensive. The reliability aspect of the devices in each application is defined by performance requirements, like the LV124 for automotive applications [1] or the IEC/PAS 62717 for general lighting [2]. These customer-defined reliability standards describe the electrical and environmental conditions, which the LED devices have to withstand. The required lifetime of the device typically depends on the weakest element in the system, which can be failure cause or/and mechanism. One example is given by solder joint fatigue, which is a typically package related failure mode, but can also be root cause for chip cracking in fact of increasing junction temperature. Typical failure modes are listed in Table 1 divided into semiconductor and package related failure mechanisms with their corresponding failure cause. The table is an adaptation for flip-chip modules from reference [3].

One of the listed standards in the performance requirement LV124 [1] is the power cycling (PC) test. In case of LEDs, it is also called supply switching test (SST) [2], which simulates the On/Off switch of LED devices like in real applications. The reliability of LED modules is mainly influenced by the thermal properties of the used interconnection and package. They are responsible for transferring the produced heat from the LED chip to the heat sink, hence they are representing the heat path of the device [4]. A change in the thermal path, like a degradation of a material, leads to an increase in thermal resistance and hence in temperature over the runtime of the PC test. The investigation concerning the utility of thermal impedance for root cause analysis as well as the improvement in the interpretation of the structure function of the thermal behaviour via thermal impedance measurement and thermal simulation are published elsewhere [5, 6]. As already mentioned, the increase of temperature in the system can cause certain failure mechanism [7], which are limiting the lifetime of an electronic system. There are already many reliability models in literature [8], which predicts the number of cycles until a certain failure mechanism occurs, but they are independent of the failure cause. However, in this paper a parametric driven monitoring model including the root cause aspect is presented. There, the initial state of the electronic device is traced by a parameter, which is linked to a failure cause, e.g. the change in temperature over the number of performed cycles until failure of the LED package. Furthermore, such models predict the lifetime at each time

* Corresponding author.
E-mail address: julien.magnien@mcl.at (J. Magnien).

https://doi.org/10.1016/j.microrel.2018.01.005
Received 10 July 2017; Received in revised form 30 October 2017; Accepted 13 January 2018
0026-2714/ © 2018 Elsevier Ltd. All rights reserved.

Table 1
Selected failure mechanisms and causes for flip-chip devices.

Mechanism	Cause	Testing method
Semiconductor-related failure mechanisms in flip-chip LEDs		
Chip cracking	High ambient temperature, high junction temperature	Thermal cycling, power cycling
Electrode cracking	High temperature gradients, CTE mismatch	Thermal cycling, power cycling
Package-related failure mechanisms in LEDs		
Solder joint fatigue	High temperature gradients, CTE mismatch, plastic deformation	Thermal cycling, power cycling, vibration test
IMC cracking	High temperature gradients, CTE mismatch	Thermal cycling, power cycling, vibration test
Delamination	High ambient temperature, CTE mismatch	Thermal cycling

under loading or in real applications by analysing the change of a certain parameter, which indicates a failure of the device. Such monitoring systems can be applied for predictive maintenance of LED modules to reduce cost and time.

In this paper, a parametric driven monitoring model was investigated to predict the lifetime of a flip-chip LED module via the change in thermal resistance, which describes the heat flow characteristics of the given system over the runtime of a PC test. The developed model describes the increase of the temperature, based on the change in thermal resistance of the device. It predicts the lifetime of the analysed LED in case of parametric monitoring during testing. Radioscopic analysis was investigated to localize the failure cause and linking them to the thermal resistance.

2. Materials and methods

The investigated LED module for the PC test consists of four blue flip-chip LEDs (Epistar, InGaN based blue emitting LED chip), which are serial mounted on a copper core PCB via SnAgCu joints with a thickness of ~40 µm. The PCB with a total thickness of 0,6 mm consists of a FR4 basis with bottom-side copper via-layer as heat transition to a heat sink. The schematic structure of the studied flip-chip LED module is shown in Fig. 1.

2.1. Power cycling test (PC)

The PC test is generally applied as a method of evaluating the fatigue life of LED modules under thermal cyclic loading [2]. It is an active temperature cycling test, where the module is actively heated by the losses, generated in the chips themselves. The device under test was mounted via a thermal interface material on an oil cooled heat sink (Julabo F25-MA) with a temperature T_s of 8 °C. A constant load current

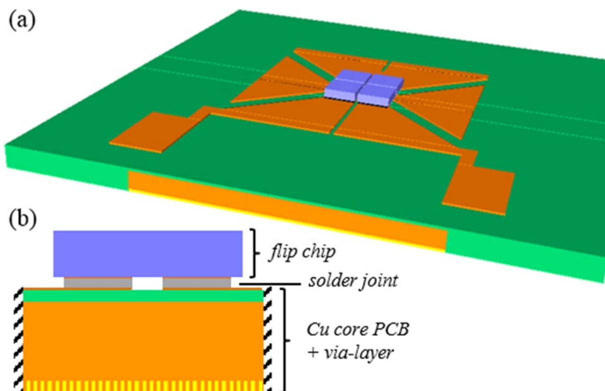


Fig. 1. Schematic structure of the module with four in serial connected blue flip-chips (a) on a copper core PCB with a via-layer on the bottom side (b).

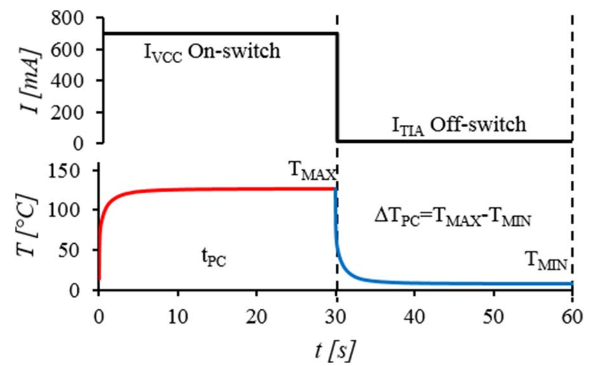


Fig. 2. Schematic On/Off-switch of the PC test with a temperature swing of $\Delta T_{PC} = 117$ °C.

(I_{VCC}) was applied by a programmable power supply (Keithley 2200-30-5) to load the LED module by the heat losses of the chips during the On-switch. The Off-switch was defined by a sense current (I_{TIA}) of some mA to avoid self-heating and the system cooled down to a minimum temperature. The sense current was applied to use the thermal impedance analysis (TIA) for monitoring the PC test over time. The applied power cycle with an electrical power of 8,25 W occurring to a temperature swing of $\Delta T_{PC} = 117$ °C, followed up by a dwell time of $t_{PC} = 30$ s. The schematic of the On/Off-switch for the investigated LED module is shown in Fig. 2. The On/Off-switch was repeated until failure of the LED module appeared.

The characteristic value for the PC test is the temperature swing ΔT_{PC}, defined by the difference between maximal temperature T_{MAX} at the end of the heating phase and the minimal temperature T_{MIN} at the end of the cooling phase. The temperature swing results in mechanical stresses in the solder joints due to the CTE mismatch of the surrounded materials. This mechanical stress leads to fatigue of the SnAgCu interconnection over the applied number of temperature cycles [9–11]. A further characteristic factor is the dwell time t_{PC}, which defines the time range and hence determines the maximum or minimum temperature. Furthermore, t_{PC} affects creep [12, 13] and aging effects [14, 15] for higher temperatures.

2.2. Thermal impedance characterization

Thermal impedance characterization was carried out by the thermal test setup from Mentor Graphics ® (T3ster) at the Off-switch, to determine the initial state of the LED module. The T3Ster monitored the temperature dependent voltage during the Off switch. Further, this signal was translated in a thermal transient, which can also be transformed in a so-called structure function. The structure function is built up of a thermal capacitance and thermal resistance (C_{th}/R_{th}) network [16–19]. Fig. 3 shows the structure function of the applied flip-chip LED module divided into different C_{th}/R_{th} sections. Each $C_{th,i}/R_{th,i}$ section can be interpreted as different elements of the LED module in the heat path down to the heat sink. A detailed information about the structure function of this four chip module was given via validated simulation and was already discussed by Mitterhuber et al. in [5, 20].

In this paper the focus was to investigate the changes in R_{th} of LED modules in terms of reliability issues. R_{th} is the ability to dissipate the internally generated heat and determines the junction temperature T_j at given heating power of the LED chip. This context was used to monitor the changes in the heat path with the parameter R_{th}. The C_{th} and the optical performance was unattended for the following thermal impedance characterization.

The analysis of the thermal transient according to the JEDEC 51–1 [21] allows the evaluation of T_j and the changes of ΔT_j over the runtime of the power cycling test. Furthermore, the calculated structure function provides information on variations in the thermal path and was

Download English Version:

https://daneshyari.com/en/article/6945752

Download Persian Version:

https://daneshyari.com/article/6945752

Daneshyari.com