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Study and analysis of DR-VCO for rad-hardness in type II third order CPLL

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ABSTRACT

In this paper, suitability of differential ring VCO designed using 90 nm CMOS process for the SET environment is studied for number of delay stages ranging from three to eleven operating at 2.6 GHz frequency. Effect of increasing the number of VCO delay cell stages to suppress SET strike sensitivity of oscillator has been studied for Linear Energy Transfer (LET) values between 20 and 200 MeV-cm^2/mg. To further validate the relation between the number of stages used in VCO architecture and SET tolerance level, the differential ring VCOs are tested within a type II 3rd order CPLL operating at the same frequency. Circuit simulations show that the PLL performance parameters: settling behaviour and error cycles of PLL are strongly correlated to the number of delay stages used in the VCO. The error cycles produced by CPLL with 11 stage VCO in response to SET hit with LET value of 200 MeV-cm^2/mg achieves 53% improvement compared to CPLL with 3 stage VCO.

1. Introduction

The performance of nanoscale CMOS circuits has improved significantly with technology scaling. However, with shrinking feature size, supply voltage and node capacitances have scaled down as well [1,2]. Reliability of electronic circuits designed to work in radiation environments such as nuclear facilities, avionics, defence and space applications has become a major concern for electronic circuit designers as the logic state of a node could be easily flipped when energetic heavy ions such as protons, neutrons or alpha particles hit the source/drain diffusion of MOSFETs. The heavy ion strikes will result in Single Event Upsets (SEU) in memory and logic circuits [3–6]. On the other hand, in analog circuits, these ionizing particles could produce Single Event Transients (SETs) in MOSFETs which will result in non-destructive effect such as transient variation in output voltage.

Phase Locked Loops (PLLs) are broadly used in mixed-signal integrated-circuits for numerous applications such as clock generation and recovery, frequency multiplication and local oscillator signal generation for mixer blocks in transceivers [7–9]. In a high-speed digital communication system, the performance of PLL is crucial for reduced bit error rate. PLL resilience is essential to reduce the vulnerability of PLL so as to reduce bit errors in clocked circuits under radiation environment. Recent researches have focused on characterizing SETs in PLL blocks for radiation hardened design. Among the functional blocks of PLL such as Phase Frequency Detector (PFD), Low Pass Filter (LP) Charge Pump (CP), and Voltage Controlled Oscillator (VCO); the CP and VCO have been identified as the most vulnerable to SETs [10–14]. To improve SET tolerance in PLL, tristate voltage based charge pump and current based charge pump using current compensation technique have been proposed in [10,11]. Radiation hardening for current starved VCO based PLL has been proposed in [12–14]. In [15] Triple Modular Redundancy (TMR) technique, majority voter circuit has been used to reduce radiation-induced jitter. Since VCO dominates the single Event (SE) susceptibility of PLL [13]; phase displacement study for LC-VCOs and different ring oscillator topologies (single ended current starved inverter based and differential ring oscillator topologies) have been extensively studied in [16,17].

In this paper, the impact of the number of delay cell stages (ranging from 3 to 11) used in differential ring VCO (DR-VCO) topology in reducing phase displacement is analysed using classical small signal model and feedback theory. The VCOs were designed using 90 nm CMOS process for a constant target frequency of 2.6 GHz and simulated in Keysight's Advanced Design System (ADS). To further validate the analysis and simulation results, the DR-VCOs of a different number of stages have been tested using type II 3rd order Charge pump based PLL (CPLL) testbed. As part of the validation, design of a third order CPLL for fast settling time post SET is considered in this paper.

2. Differential ring oscillator

The four-stage differential delay cell-based ring oscillator topology with inversion in the third stage for oscillation to occur (no inversion required for the odd number of stages) is shown in Fig. 1a. Unlike, single ended current starved delay cell based VCO which need to have

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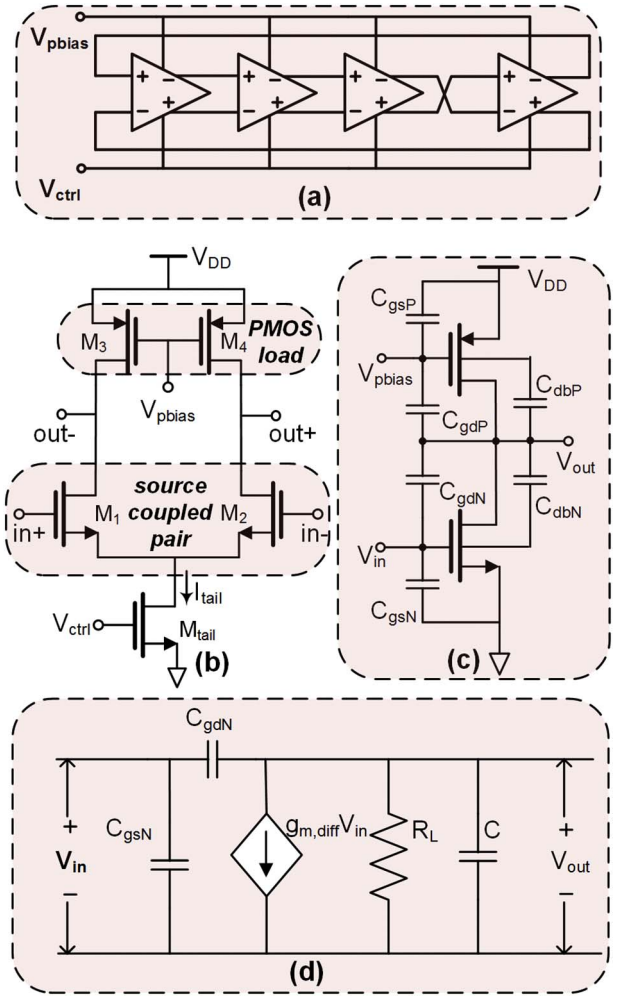

Fig. 1. (a) 4-stage differential ring oscillator topology (b) differential delay cell used in VCO (c) common source delay stage with parasitic capacitances of one limb of differential cell, and (d) small signal equivalent circuit of a common source stage.

an odd number of stages, the differential delay cell of the DR-VCO can have odd or even number of stages. The differential delay cell shown in Fig. 1b is used for analysing the behaviour of DR-VCO and DR-VCO based CPLL. The delay cell consists of a differential pair M1, M2 (alternately M_{DIFF}), PMOS load M3, M4 (alternately M_{LOAD}) biased with gate voltage V_{pbias} and a tail transistor M_{tail} with tail current I_{tail}. The frequency of oscillation is controlled by varying the tuning voltage V_{ctrl}. Assuming virtual ground at the source terminals of the differential pair M1 and M2, common source configuration of one end of the DR-VCO delay cell stage with parasitic capacitances is shown in Fig. 1c. The gate to source, gate-drain and drain-bulk capacitances of PMOS load is represented by C_{gsP},C_{gdP} and C_{dbP} respectively. Similarly, C_{gsN},C_{gdN} and C_{dbN} represents gate to source, gate-drain and drain-bulk capacitances of NMOS common source differential pair.

The small signal model of the common source stage for one end of differential delay cell is shown in Fig. 1d. The transconductance of the differential pair and load resistance are represented as $g_{m.diff}$ and R_L respectively. C is the sum of drain diffusion capacitances (C_{dbN}, C_{gdN}, C_{gdP}, C_{dbP}) of M_{DIFF}, M_{LOAD} and the gate capacitance of the differential pair which is basically $C_{ox}W_{DIFF}L_{DIFF}$ where W_{DIFF} and L_{DIFF} are the width and length of the differential pair M_{DIFF}. $R_L = 1/(\lambda_p + \lambda_n)\cdot I_{tail}$ where λ_p and λ_n are the channel length modulation parameters of M_{DIFF} and M_{LOAD} respectively.

2.1. Small signal and large signal frequency of a differential cell

The transfer function of the common source small signal equivalent circuit shown in Fig. 1d is given by

$$a_m(j\omega) = \frac{-g_{m,diff}R_L + j\omega R_L C_{gdN}}{1 + j\omega R_L C} \tag{1}$$

Since every stage in the ring oscillator is identical, it has same transfer function as given by Eq. (1). Thus, for an m-stage VCO, the transfer function follows Eq. (2).

$$T_{VCO}(j\omega) = (a_m(j\omega))^m = \left(\frac{-g_{m,diff}R_L + j\omega R_L C_{gdN}}{1 + j\omega R_L C}\right)^m \tag{2}$$

The small signal oscillation frequency of an m-stage oscillator depends on phase condition of the $T_{VCO}(j\omega)$. Solving for arg $(T_{VCO}(j\omega)) = -\pi$, gives the phase relation as

$$\tan^{-1}\left(\frac{\omega_{m,ring}C_{gdN}}{g_{m,diff}}\right) + \tan^{-1}(\omega_{m,ring}R_L C) = \frac{\pi}{m} \tag{3}$$

Since the transistor transition frequency $g_{m.diff}/C_{gdN} < < R_L C$, the oscillation frequency $\omega_{m,ring}$ of ring oscillator can be simplified as

$$\omega_{m,ring} = \frac{1}{R_L C}\tan\left(\frac{\pi}{m}\right) \tag{4}$$

This small signal frequency expression in Eq. (4) is fairly true for oscillation startup. However, as oscillation grows up the device nonlinearity limits further oscillation growth. In that case, large signal frequency analysis is better suited for frequency analysis. Using differential slew rate I_{tail}/C and output voltage swing V_{sw} of the delay cell, the large signal frequency for m-stage VCO can be given as [18].

$$f = \frac{I_{tail}}{2m\cdot C\cdot V_{sw}} \tag{5}$$

2.2. Phase displacement in VCO due to SET

2.2.1. SET current model

Any radiation ion strike at the reverse biased drain-bulk junction of the MOSFET generates free electron-hole pairs in the depletion region. The SET current I_{SET} generated by these excess electron-hole pairs is modelled using double exponential current source [19,20].

$$I_{SET} = \frac{Q_{SET}}{\tau_\alpha - \tau_\beta}\left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}}\right) \tag{6}$$

$$Q_{SET} = 10.8^{*}L^{*}\text{LET} \tag{7}$$

where Q_{SET} is the amount of charge deposited by a particle track, L is the charge collection depth (L is approximately 1 μm for 90 nm technology) and LET is the Linear Energy Transfer in units of MeV-cm^2/mg. The collection time constant τ_α and ion track establishment time constant τ_β of the pulse is chosen as 164 ps and 20 ps respectively [17]. In this is work, Eq. (7) is deduced from [17] and is specific to the proposed design.

2.2.2. SET impact in DR-VCO

In DR-VCO delay cell shown in Fig. 1b, the tail transistor nearly acts as a constant current source with tail current I_{tail} in the entire oscillation cycle, whereas the current in differential pairs varies in the range (0, I_{tail}) due to its switching nature. This switching behaviour of differential pair makes it more susceptible to ion strike compared to the tail transistor. Since the output is taken from the drain nodes of the differential pair, it is more vulnerable to heavy ion strike. Any SE strike deposits a charge Q_{SET} at the output node of the differential delay cell. Until Q_{SET} is dissipated from the hit node, amplitude and phase perturbation occurs in the oscillator. Momentary increase or decrease in oscillating