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NBTI: Experimental investigation, physical modelling, circuit aging simulations and verification

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ABSTRACT

For more than 10 years a major part of MOSFET reliability publications are dealing with (N)BTI. The degradation and recovery mechanism is still not fully understood (Grasser, 2014). New publications demonstrate incessantly the agile debate on this important transistor aging phenomenon.

In this paper we want to illuminate four important subareas for the understanding of NBTI. First, we will discuss experimental investigations. Depending on the pursued goal of the measurements different set-ups are required to gain the desired information. To get meaningful statements regarding the median NBTI degradation of MOSFET with a relatively small number of test devices, e.g. for regular lifetime predictions, DUTs with larger active area are used. The relatively high number of defects within one transistor delivers stable (averaged) parameter shifts with a small number of DUTs. Relatively small area devices are the best choice to investigate the physical nature of the degradation and recovery mechanisms. The small number of defects within those devices enables to obtain and investigate the trapping and de-trapping of single charges. To investigate the NBTI impact on the parameter variability array structures with a higher number of devices under test (DUTs) are appropriate. The very fast and strong recovery behavior of NBTI has to be considered for the test structure design and for the measurement set-up.

Based on the measurement results and gained knowledge we can refine the modelling of the degradation and recovery mechanism. We could improve the understanding of the temperature dependence and utilize this knowledge to reduce measurement efforts for model calibration for a circuit aging simulator (Pobegen and Grasser, 2013). An adequately accurate model at a manageable effort for characterization and implementation is a key factor for a successful integration of an aging simulator in the design flow. A correct modelling of the parameter recovery during circuit function is especially challenging.

The last chapter introduces a new method to verify the NBTI model and the correct implementation into a circuit aging simulator with real hardware measurements. An arbitrary waveform generator is used to drive single transistors in identical operation modes with identical sequence and proportion of each single operating point as during real circuit operation. In this manner, the calculated drift for one transistor in a circuit can be compared with a measurement drift for a given stress pattern.

1. Large area DUTs for simple lifetime predictions

For regular lifetime prediction based on accelerated stress measurements the JEDEC BTI guideline [3] proposes to test transistors with large active area. For example a geometry of W = 10 µm and L = nominal channel length of the investigated technology. An upper limit for high W/L ratios is given by possible IR-drop problems of the test-structure and contacts due to large currents (for characterization).

A relatively large active area of the test-transistors leads to a high number of active defects regarding (N)BTI degradation. The influence of a single trapped charge decreases with larger active area. The channel shows low RTN disturbance [4]. The variability of the electrical parameter of those devices is much smaller in contrast to devices with smaller areas. The standard deviation is smaller for virgin devices and even the variability of the NBTI induced parameter is smaller. Therefore, DUTs with larger active area are predestined to investigate averaged values (before and after degradation) as required for regular lifetime estimation based on a relatively low number of test-devices.

2. TDDS

Small area devices provide the clearest insight into the physic of

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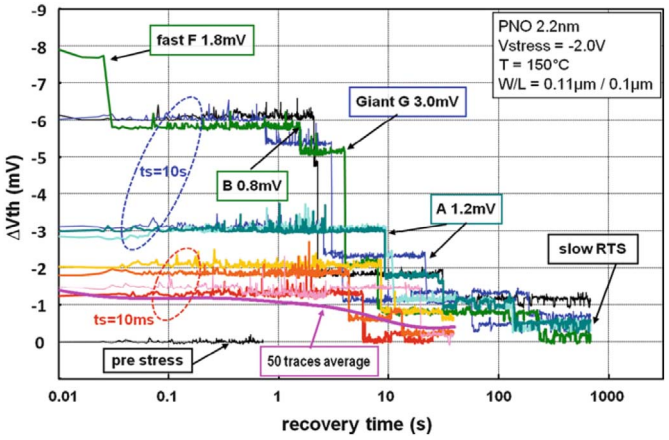

Fig. 1. Recovery traces recorded after repeated gate stress pulses with t_s = 10 ms and 10 s pulse length. Four different defects (named A, B, F, G) with different capture- and emission-time constants and step heights are charged. Also shown is an average over 50 recovery traces after t_s = 10 ms, showing the exponential distribution.

charge trapping and de-trapping during degradation and recovery. The active area of the test transistors has to be small enough to conveniently resolve the effect from a single carrier in the channel (typical ΔV_{th} = 1 mV) and large enough to have at least a handful of active defects ($\approx$ 20 average step-height defects for ΔV_{th} = 20 mV). We achieved the greatest advances in NBTI understanding with this kind of DUTs [5]. The development of the time dependent defect spectroscopy (TDDS) has revolutionized the modelling of NBTI [6–9].

The TDDS technique is in principle an extension of the deep level transient spectroscopy (DLTS) adapted to small area FETs [10]. Since capture time constants have a wide distribution, it is essential to vary the length of the charging pulses. This is why we term the technique time dependent defect spectroscopy (TDDS). The purpose of TDDS is to extract the properties of single, individual defects in MOSFETs, the capture and emission time constants τ_c and τ_e (corresponding to stress and recovery), the temperature- and field-dependencies of those τ_cs and τ_es, and thus to gain insight in physical processes. To achieve a highly accurate determination of averaged time constants, the values are extracted from repetitive measurements.

Fig. 1 shows an example for a TDDS measurement, using a pMOSFET with SiON gate oxide. The stress pulses applied prior to measuring the recovery traces had two different lengths, i.e., 10 ms and 10 s, and about 7 (equivalent) recovery traces are shown after each stress condition. A couple of important things can be seen in Fig. 1: Four defects can be analyzed simultaneously from the data shown in Fig. 1. Each defect is characterized by its individual step height in V_{th}, which is like a *fingerprint* of the corresponding defect. This is of utmost importance for the analysis of a given defect.

The TDDS technique has proven to be a powerful technique for the characterization of border traps in MOSFETs. Besides electron spin resonance [11], electrical techniques probing the properties of single defects like RTS or TDDS are the only methods having the potential to reveal direct information on the physical nature of defects in gate oxide and interface. The TDDS technique is still in use for further exploration of the damage mechanisms.

With the help of TDDS, the following conclusions based on experimental observations can be summarized [1,12]:

1. NBTI degradation and recovery have been shown to be due to charging and discharging of individual defects with a wide distribution of timescales. Both capture- and emission-time constants are temperature activated with activation energies E_A in the order of 1 eV, consistent with nonradiative multiphonon theory. Furthermore, the time constants are uncorrelated and can be very long ($> 10^5$ s) in thin oxides as well. No signs of a temperature-independent elastic tunneling process could be found. The defects responsible for the recoverable component of NBTI are identical to those causing RTS [13].
2. The capture-time constants show very strong field dependence. Similarly, the bias dependence of the emission-time constant around V_{th} may be either weak or strong, depending on the configuration of the defect.
3. It has been shown that oxide defects can be volatile [14]. They can transform and change their properties. Still, the simple two-state model as represented by stationary CET-maps is a reasonable approximation. The total number of defect precursors is preexisting and hardly any signs of newly created defects could be found in short- to medium-term stress experiments at standard NBTI stress fields.
4. The existence of metastable states becomes obvious due to disappearing defects and transient RTS, and in anomalous AC behavior. Thus real defects are more complicated than simple “two-state defects.”
5. TDDS results show that even for long-term stress times > 100 s, the recovery time for any given trap is independent of the preceding stress time, thus excluding degradation or recovery governed by diffusion [15].
6. TDDS yields a correct determination of activation energies E_A, in contrast to standard experiments with wide FETs.
7. The analysis of TDDS step heights [16] helps to get a deeper understanding of variability of BTI degradation, which is important for SRAM failure and analog circuits.
8. The concept of universal recovery of NBTI which has been shown to be approximately in agreement with experimental data [17], is not supported by findings from TDDS.
9. The power law exponent n, describing NBTI degradation as $\Delta V_{th} \propto t_s^n$, with n around 0.15, has its origin in the distribution of capture-time constants rather than being controlled by diffusion of a hydrogen species in the gate stack.

These findings from TDDS play an important role for the TCAD model and for the justification of the simplified capture and emission time map (CET-map) model to be treated in the modelling section.

3. Time dependent variability

Small area devices, as used for TDDS measurements, show distinct statistical parameter variations and NBTI influences the parameter distribution. Variability and reliability of MOSFETs interact. Stress induced electrical parameter degradation of MOSFETs over lifetime and the variability of those parameters cannot be considered separately. The parameter variability is impacted by aging; the degradation itself shows a distribution. Accordingly parameter variability is time-dependent [19].

The parameter variability of MOSFETs can degrade over lifetime. E.g. the distribution of the threshold voltage V_{th} after NBTI stress originates from a convolution of the distribution of the virgin devices together with the additional distribution of the BTI degradation itself. Later on we will demonstrate that the variability can also recover.

Fig. 2 sketches the situation. The variability of V_{th} of the virgin devices is based on process induced random distribution of dopant atoms, gate oxide thickness, channel length, line edge roughness etc. [18]. Already in the late 1980s several publications discussed the variability of MOS transistors [19–22], in particular for matched or exactly weighted transistors in basic analog blocks like current mirrors or differential stages for amplifiers or comparators. The accurate function of those circuits relies on the exact matching of two (input-) devices. Large active areas and other layout measures can reduce the variability of device parameters at zero hour [23]. However, what helps to mitigate degradation induced mismatch during lifetime? The risk for such an asymmetrical degradation of matched or weighted devices